UCLA Computer Science Department: CS M51A / EE M16 Prof. Miloš D. Ercegovac
Logic Design of Digital Systems Engineering VI 468B
Fall 2019, TR 8:00 - 9:50am, Bunche Hall 1209B 825-5414; e-mail: milos@cs.ucla.edu
Office hours: Engineering VI, 468B, Tue 2:00pm - 3:00pm, or by appt. http://www.cs.ucla.edu/~milos

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Course material: Lecture viewgraphs and class notes; readings; solutions; sample exams will be posted on the **CourseWeb**.
Textbook: M.D. Ercegovac, T. Lang and J. Moreno, *Introduction to Digital Systems*, John Wiley & Sons, New York, 1999. Available as reader at UCLA Bookstore and on the Web.

Grading: Homeworks 10%, quizzes 20%, midterm 30%, final 40% .
TAs: Dis 2A - A.Verma; Dis 2B - A. Joshi; Dis 2C - H. Zhu; Dis 2D - V. Malik
• **Homeworks must be turned in at the beginning of discussion sessions - no exceptions!**
• **LogiSim Design Tool:** used in discussion sessions. LogiSim is an easy to use schematic editor and logic simulator; free download at **LogiSim**.

CS M51A Fall 2019: Syllabus and Schedule

Week 1

- Thursday, 9/26. About digital systems. Combinational and sequential systems. Specification, design, and analysis of systems. Hierarchy of levels in specification, analysis and design: algorithmic (computational), register-transfer level (RTL), logic level, circuit (transistor - physical) level.
  Readings: Chapter 1.

  Specification of combinational systems. High-level and binary-level specifications. Data representation: numbers, characters, and sets.
  Readings: Chapter 2.

  Friday, 9/27, Discussion: Binary and decimal number systems and conversions. Boolean Algebra. (Appendix A).

  HW1 posted.

- Tuesday, 10/1. Combinational systems: Binary specification of inputs/outputs and functions. Central concept of functional description: switching function (SF). Incompletely specified SFs. Basis of hierarchical specification and design: Composition of SFs. Switching algebra, switching expressions (SEs, evaluation of SEs, equivalent SEs, and algebraic transformations of SEs. Standard forms for SEs: sum of products (SOP) and product of sums (POS).
  Readings: Chapter 2, Appendix A.

Week 2

- Thursday, 10/3. Canonical forms: Sum of minterms and product of maxterms. Examples of combinational system specifications. Readings: Chapter 2.

  Friday, 10/4,**HW1 due.** Discussion of Lectures 1 and 2.

- Tuesday,10/8. Physical level: CMOS transistor switches and gates: NOT, NAND/NOR, AND/OR, and XOR.
  Readings: Chapter 3.
  Sample Quiz 1 posted + solutions.

Week 3

- Thursday, 10/10. Complex gates. Transmission gates and their use. Timing parameters, load, load factors, and propagation delays. Three-state drivers and buses. VLSI design styles and packaging.
  Readings: Chapter 3.
  HW2 posted.
  Friday, 10/11: **QUIZ No.1. Discussions**

- Tuesday, 10/15. Gate networks definition and description. Universal gate sets. Functional analysis. Timing analysis. Logic levels and critical path. Readings: Chapter 4.

Week 4

- Thursday, 10/17. Design of combinational systems: minimal two-level networks. Graphical minimization of expressions (Karnaugh Maps).
  Readings: Chapter 5.

  Friday, 10/18:**HW2 due. Discussions.**

- Tuesday, 10/22. NAND and NOR networks. Programmable logic arrays (PLAs). Readings: Chapter 5. Examples of designs.
  HW3 posted.
  Sample Quiz 2 posted + solutions.

Week 5

- Thursday, 10/24. Synchronous sequential systems. Main types of sequential systems: Moore and Mealy Machines. Finite-state machines (FSM). State description: state table and state diagram. Time behavior. Finite memory machines. Readings: Chapter 7.
  Friday, 10/25: **QUIZ No. 2**. Discussions

- Tuesday, 10/29. Reduction of the state set. Binary specification and types of sequential systems.
  Sample Midterm posted + solutions.

Week 6

- Thursday, 10/31. Implementation of sequential systems: sequential networks. Canonical form: Huffman-Moore. Latches and Edge-triggered cells. D flip-flop. Timing characteristics. Readings: Chapter 8.

  Friday, 11/1: **HW3 due**, Discussion.

- Tuesday, 11/5. **MIDTERM EXAM** – in class –
  The exam covers Chapters 2, 3, 4, and 5. Closed books and notes. Four cheat sheets allowed. Tables and identities given if needed.

  Sample Quiz 3 posted + solutions.

Week 7

- Thursday, 11/7. Analysis and design of canonical networks. Flip-flops: SR, JK, and T. Analysis of sequential networks with flip-flops. Readings: Chapter 8.
  HW4 posted.

  Friday, 11/8: **Discussion.**

- Tuesday, 11/12. Design of sequential networks with flip-flops. Excitation functions. Special state assignments: "one flip-flop per state" and shifting register. Examples.

  Readings: Chapter 8.

Week 8

- Thursday, 11/14. Chapter 8 (cont.) Readings: Chapter 8.
  Friday, 11/15:**Quiz 3 (Chapters 7 and 8). Discussion.**

- Tuesday, 11/19. Chapter 8 (cont.) Standard combinational modules and networks - Introduction.
  Readings: Chapter 8 and Chapter 9.
  Sample Quiz 4 posted + solutions.

Week 9

- Thursday, 11/21. Decoders and Encoders. Implementation and uses. Large decoders: coincident and tree. Readings: Chapter 9.

  Friday, 11/22: **QUIZ 4 (Sections 8.7,8.8, 8.9 and 8.10). HW4 due.** Discussion.

- Tuesday, 11/26. Multiplexers, implementation and uses. Large multiplexers. Demultiplexers, implementation and uses. Shifters, types, and implementations. Uses of standard modules.
  Readings: Chapter 9.
  Sample Final - replaces HW5 - do not turn in

Week 10

- Tuesday, 12/3. Arithmetic combinational modules. Addition of positive integers. Binary adders and basic modules: Full adder and half adder. Carry-ripple adder. Representation of signed integers: Two's complement and ones' complement systems.
  Readings: Chapter 10.
  Solutions to Sample Final posted.

- Thursday, 12/5. Standard sequential modules and networks: registers, shift registers, and counters. Their specifications, implementations, implementation of larger modules, and uses.
  Readings: Chapter 11.

  Friday, 12/6: Discussion.

- **FINAL EXAM**, December 10, Tuesday, 3:00 - 6:00pm, Broad Art Center 2160E. The problems will be on the material in Chapters 7, 8, 9 (except Sec. 9.3), Chapter 10 (Sections 10.1 (skip subsection "Module Propagate and Generate Signals"), 10.2 (skip subsection "Carry-lookahead Adder Network") , and 10.3), and Chapter 11 (Sections 11.1, 11.2, and 11.3 up to "counter as the state register") . However, the exam is comprehensive, i.e., you need to know material covered in Chapters 2, 3, 4, and 5. Closed textbook and notes. Four cheat sheets allowed. Tables provided if needed.
