

Zohreh Karimi

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Objective

"An Internship job for Summer 2008"

Education

- 2006-present Ph.D student in Computer Science at University of California, Los Angeles, USA
Major: Theory
Advisor: Prof. Majid Sarrafzadeh
- 2001–2004 M.Sc. in Computer Architecture, University of Tehran, Iran
Thesis: "HW-SW Self-Testing of Processor Cores"
Advisor: Prof. Z. Navabi
- 1997–2001 B.Sc. in Computer Engineering, Hardware Major, University of Tehran, Iran
Final Project: "VHDL Synthesizability Check With XSL"
Advisor: Prof. Z. Navabi

Research Interests

- Physical Design and Placement
- Power Aware Placement
- Manufacturing Test and Design for Testability
- Computer Architecture
- HW/SW Co-design of Embedded Systems
- Reconfigurable Computing
- Sensor Networks
- EDA Tools and HDLs

Technical Skills

- **Hardware Description Languages:** VHDL, Verilog, SystemC
- **Hardware Design:** Logic Design Using Field-Programmable Devices (Altera and Xilinx devices)
- **Technical Tools:** ModelSim, MaxPlusII, LeonardoSpectrum, Xilinx ISE and EDK Tools, Quartus II, SPICE, Silos, Magma BlastFusion router, Avrora, QCADesigner
- **Programming Languages:** C++, Pascal, Assembly Programming (8086, 8051, 8085, Z80), XML, XSL, Network Programming Using TCP/IP, Servlet Programming, SQL

Work Experiences

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|------------------------------------|----------------------------|---|
| 2006-present
Research Assistant | ER Lab, UCLA | Research work on VLSI physical design, Low power placement, Low cost technology mapping |
| 2007
Summer Intern | Synplicity Inc., Sunnyvale | Congestion reduction, improved quality of results in physical design flow |
| 2002-2005 | UT CAD Research Group, | Design and implementation of a VHDL to |

Researcher, Developer and Team Manager	Tehran, Iran	SystemC converter tool
2000, July-December Summer Internship	Iran Tele-communication Research Center	Design and implementation of an interface for a voice mail system targeting Altera programmable devices using VHDL
1999, Fall Part Time Employee	UT CAD Research Group, Tehran, Iran	Testing a digital simulation engine and environment

Academic Experiences

2006, Summer, Fall 2007	Teaching Assistant, UCLA	CS152A (Digital Design Lab.), CS152B (FPGA Design Project Lab.)
2004, Fall	Teaching Assistant	Graduate course of "Digital System Synthesis"
2001-2004, four terms	Teaching Assistant	"Digital Electronics Lab."
1999, Spring	Teaching Assistant	"Digital Logic Design"

Academic Projects

2006, Winter	Physical Design	Reducing routing congestion in physical design using white spaces
2002, Spring	Test and Design for Testability	Implementing concurrent fault simulator, test pattern generator and testability measurement engines Inserting scan and BIST to SAYEH processor
2002, Spring	Computer Arithmetic	Developing and comparison of several architectures of adder/subtractors, multipliers and dividers
2001, Spring	VHDL	Implementation of V8-URISC processor in VHDL
2000, Fall	VLSI	Automatic layout generation from behavioral description of PARWAN processor using LeonardoSpectrum and TannerTools
1999, Fall	Computer Architecture	Modeling and implementation of MIPS processor in Verilog

Graduate Level Courses

Computer Architecture	CAD	Theory
Reconfigurable Computing	VHDL	Perfect Graphs
Advanced Computer Architecture	Testing and Testable Design	Online Algorithms
Bio-computing	Synthesis of Digital Designs	Graph Network Algorithms
Video Processors		Distributed Algorithms
Computer Arithmetic Algorithms		
Advanced VLSI Circuits		

Undergraduate Courses

Digital Logic Circuits	Digital Electronics	Algorithms
Computer Architecture	VLSI	AI
Computer Aided Design	Microprocessor	Databases

Awards and Honors

2006	Recipient of departmental award to participate in Grace Hopper Conference
2006-2007	Holding UCLA Graduate Division Tuition Fellowship
2004	Ranked 2 nd in the M.Sc. program among 10 students
2001	Ranked 11 th in IRAN "National Entrance Examination for Higher Education" in hardware major, among about 5000 computer-engineering graduate participants
2001	Ranked 2 nd in 1997-2001 B.Sc. calendar years
1997	Ranked 42 nd in the first stage and 131 st in overall among more than 500,000 student participants in the "National Entrance Examination" for B.Sc. program

Papers

- S. Nakatake, Z. Karimi, T. Taghavi, and M. Sarrafzadeh, "*Block Placement to Ensure Channel Routability*" ACM Great Lakes Symposium on VLSI (GLSVLSI), 2007.
- E. Safi, Z. Karimi, M. Abbaspour and Z. Navabi, "*Utilizing Various ADL Facets for Instruction Level CPU Test*," Microprocessor Test and Verification Workshop, 2003, 38-43.
- E. Safi, R. Saberi, Z. Karimi and Z. Navabi, "*Processor Testing Using an ADL Description and Genetic Algorithms*," International Conference on Very Large Scale Integration of System-on-Chip, 2003, 186-190.
- R. Saberi, E. Safi, Z. Karimi and Z. Navabi, "*Controller Testing Using Combination of GAs and Symbolic Methods*," Workshop on RTL and High Level Testing, 2003, 49-54. (also as presenter)
- Z. Karimi, H. Farshbaf, E. Safi and Z. Navabi, "*A Pluggable Environment for Evaluation of RT Level Hardware Component Designs*," International Conference on Simulation and Multimedia in Engineering Education, 2002, 35-42.
- Z. Karimi and Z. Navabi, "*VHDL to SystemC Translation for Hardware-Software Co-Simulation*," International Symposium on Telecommunication, 2003, 237-240. (also as presenter)

Misc.

- T. Taghavi, Z. Karimi, and M. Sarrafzadeh, "Wirelength Estimation for Large Scale Circuits in the Presence of Blockage," Embedded and Reconfigurable System Lab., CS Dept. Research Review, UCLA, May 2006.
- Z. Karimi, M. Sarrafzadeh, "*Low Cost Clustering under Timing Constraint*", under submission.
- Z. Karimi, M. Sarrafzadeh, "*Voltage Island Aware Placement*", under submission.

References

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