

Curriculum Vitae

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Education: Ph.D. degree (1975) and M.S. degree (1972) in Computer Science, University of Illinois, Urbana-Champaign, Illinois; B.S. degree (1965) in Electrical Engineering, University of Belgrade, Belgrade, Serbia.

Ph.D. Dissertation: *A General Method for Evaluation of Functions and Computations in a Digital Computer* (U. of Illinois, DCS Technical Report No. 750, 1975).

Ph.D. Committee: James E. Robertson (Chair), David J. Kuck, Chuang L. (Dave) Liu, Donald B. Gillies, and Ahmed Sameh.

Professional Experience: Distinguished Professor (2010 - present), Computer Science Department, HSSEAS, UCLA;
Professor (1984 - 2010), Computer Science Department, HSSEAS, UCLA;
Department Chair (9/1/2000 - 6/30/2005);
Vice-Chair (Graduate Programs) (1995-1998, 1988-1994, 1982-1986);
Vice-Chair (Industrial Relations) (1998-1999, 2009 - present);
Associate Professor (1979-1984);
Assistant Professor (1975-1979);
Research Engineer (1966-1970), Institute for Automation and Telecommunications "M.Pupin," (Digital Laboratory), Belgrade, Yugoslavia;
Assistant Engineer (1965-1966), Brown Boveri Co., Telecommunications, Baden, Switzerland;
Consultant to: Hughes Research Laboratories, (1979-1990); Jet Propulsion Laboratory, (1978-82); U.S. government and industrial organizations (1975 - present); GMD Institute (German government), (1984-88). Hughes Aircraft Company, (1988 - 1997).

Research Theory and design of computer arithmetic algorithms: emphasis on fast division, square root and multiplication; design of fast floating-point units; complex arithmetic; on-line arithmetic, most-significant-digit-first algorithms, and composite algorithms; arithmetic structures for low power; application-specific numerical processors; reconfigurable gate arrays (FPGAs) and systems; functional (applicative) languages and architectures; digital design.

Teaching UCLA Computer Science Department: *Logic Design of Digital Systems* (CS M51A), *Computer Systems Architecture* (CS151B), *Design of Digital Systems* -

Elective (CS151C), Advanced Computer Architecture (CS251A), Parallel Computer Architecture (CS251B), Arithmetic Algorithms and Processors (CS252A), Special Topics in High-Speed Computing (CS259 - Seminar);
 UCLA Extension: *High-Speed Computer Organization: Super Machines and Low-Cost Systems*, Short Course, (1979 - 1986).

Membership and Professional Services

- Foreign Member, Serbian Academy of Sciences and Arts, (2003 - present);
- Fellow IEEE (2003 - present);
- IEEE Computer Society (1975 - present); IEEE Technical Committee for VLSI for Signal Processing;
- ACM (1975 - present); SigARCH;
- Nikola Tesla Memorial Society, Science Committee (1985 - present);
- UCLA Engineer Advisory Board, 2001 - 2004;
- Chancellor's Advisory Board for the Crump Institute (UCLA Medical School) (1985 - 1995);
- IEEE Transactions on Computers, Editorial Board (1988-1992); • Journal of Parallel and Distributed Computing, Editorial Board (1986-1993);
- Program Committee of the IEEE Symposium on Computer Arithmetic (1978 - present); General Chair (1978); Program Co-chair (1989);
- Chair, IEEE Steering Committee on Computer Arithmetic (1999 - 2001); Member (1999- present);
- Technical Program Co-Chair, IEEE ASAP 2009. (Application-Specific Systems, Architectures and Processors);
- Member, Asilomar Conference on Signals, Systems and Computers, Steering Committee (2004 - present);
- Arithmetic Session Chair, ASILOMAR Conference, (1986, 2004, 2006, 2007);
- Arithmetic Session Chair, SPIE Conference, (1999-2001, 2003, 2004, 2009);
- Member, Technical Program Committee, FCCM, 2007 - present;
- Member, Technical Program Committee, RNC'5 (Real Numbers and Computers), 2003.

Invited Seminars and Panels

- Omnipresence of Tesla's Work and Ideas, Electrical and Computer Engineering Department, Yale University, September 7, 2010;
- Getting More from Less: Trends in Computer Architectures, Serbian Academy of Sciences and Arts, Belgrade, September 19, 2007;
- Omnipresence of Tesla's Work and Ideas, Simon Fraser University, Burnaby, Canada, November 17, 2006;
- Omnipresence of Tesla's Work and Ideas, Serbian Academy of Sciences and Arts, Belgrade, October 18, 2006;
- Arithmetic Approaches to Bayesian Network Computations, Intel-Barcelona Lab, July 8, 2005;
- On-line Arithmetic, STMicroelectronics Lab, San Diego, August 11, 2004.
- New Models for Computer Engineering Programs, CRA Conference at Snowbird, July 12, 2004.
- Complex Arithmetic, Microsoft Research Lab, April 21, 2004;
- Fast Low-Power Multipliers, EE Department, University of Belgrade, Serbia, June 2003;
- Complex Division with Prescaling of Operands, ECE Department, University of Wisconsin - Madison, March 2003.
- Fast Arithmetic, ECE Department, George Washington University, Washington, D.C., March 2001.
- Seminar on Nikola Tesla, UC Berkeley, 2000.
- Reconfigurable Arithmetic Seminar, University of Provence, Marseilles, France,

June 1999.

- Online Algorithms, Symposium on CORDIC, Technical University, Delft, Holland, March 1998.
- Redundant Arithmetic, Seminar, University of Provence, Marseilles, France, June 1998.
- Online Arithmetic, 12th Symposium on Weak Arithmetic, Metz, France, 1996.
- Approaches to Fast Arithmetic, Real Numbers and Computers, St. Etienne, France, 1995.
- Low-Power Arithmetic, University of California at Los Angeles, Computer Science Department Seminar, 1994.
- Arithmetic for Recursive Filters, Rockwell International Science Center, Thousand Oaks, May 1993.
- Online Arithmetic: Design Methodology and Application, 1992 IEEE Workshop on VLSI Signal Processing, Napa, 1992.
- Fast Arithmetic, **Distinguished Speaker**, EE Department, UC San Diego, 1991.
- On-Line Arithmetic, Ecole Normal Supérieure , Lyon, France, 1991.
- Application-Specific Arithmetic Approaches, University of California at Los Angeles, Computer Science Department Seminar, 1990.
- Composite Arithmetic, University of California at Santa Cruz, Computer Science Program Seminar, 1990.
- Vector Processors, ETAN Advanced Simulation Seminar, Dubrovnik, 1990.
- High-Performance Computer Architectures, Lecture Series, Institute M. Pupin, Belgrade, 1989.
- Supercomputers, Annual Computer Society Conference, Rio de Janeiro, Brazil, 1988.
- Redundant Arithmetic, Memorial University, New Foundland, Canada, 1988.
- Fast Arithmetic, USC, EE & Systems Department Seminar, 1987.
- Parallel Architectures, Eidgenössische Technische Hochschule (ETH) Seminar, Zuerich, Switzerland, 1987.
- Supercomputer Architectures, Technical University of Berlin Seminar, 1986.
- On-Line Arithmetic and Dataflow Architectures, University of Utah, Computer Science Department Seminar, 1985.
- High-Performance Architectures, Gesellschaft fuer Mathematische Dataverarbeitung, St. Augustin-Bonn, Germany, 1984;.
- On-Line Arithmetic Algorithms, Yale University, Computer Science Department Seminar, 1983.
- Evaluation of Polynomials and Rational Functions, Ecole Supérieure d'Electrotechnique et Electronique Seminar, Paris, 1983.
- Low-Cost Processors, Special Libraries Association, Los Angeles, 1982.
- Panel, IEEE Workshop on Computer Elements, Phoenix, 1982.
- Approaches to High-Performance Architectures, Invited Speaker DATASHOW'81, Tokyo, 1981.
- On Supercomputer Architectures, Institute for Automation "M.Pupin," Belgrade, 1981.
- Dataflow Architectures, Electrical Engineering Department, University of Belgrade, 1981.
- Floating-Point On-Line Arithmetic, University of Michigan, 1980.
- Short Course on Computer Organization, IBM Santa Teresa Labs, 1979.
- A Method for Evaluating Rational Approximations, ACM SIGNUM Los Angeles Chapter Seminar, 1978.
- Panel, MIT Data-Flow Workshop, 1977; MIT Data-Flow Workshop, 1978.
- Online Iterative Networks, University of Michigan, Electrical and Computer Engineering, 1976.

- Digital Arithmetic - Some New Results, Electrical Engineering Department, University of Belgrade, 1976.

Awards

- The Lockheed Martin Excellence in Teaching Award, 2009.

- The Okawa Foundation: Efficient Schemes for Fast Computation of Inferences in Bayesian Networks, 2006.

- Best paper award: M.D. Ercegovic and J.-M. Muller, Complex Square Root with Operand Prescaling. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2004.

- Foreign Member of the Serbian Academy of Sciences and Arts, for contributions to theory and practice of digital arithmetic, 2003.

- IEEE Fellow, for contributions to theory and practice of digital arithmetic, 2003.

- NASA Certificate of Recognition for technical contributions to fault-tolerant computer systems, 1980.

Books, Chapters in Books, and Editorships

1. F. de Dinechin, M. D. Ercegovic, J.-M. Muller, and N. Revol, *Digital Arithmetic*, Chapter in: Wiley Encyclopedia of Computer Science and Engineering, Benjamin Wah (Ed.), New York: John Wiley & Sons, Inc., 935-948, 2008.
2. M.D. Ercegovic and T. Lang. *Digital Arithmetic* Morgan Kaufmann Publishers - an Imprint of Elsevier Science, San Francisco, 2004.
3. M.D. Ercegovic, T. Lang and J. Moreno, *Introduction to Digital Systems.*, John Wiley & Sons, (translation in Chinese), pps. 498, 2002.
4. M.D. Ercegovic, T. Lang and J. Moreno, *Introducao aos Sistemas Digitais.*, Porto Alegre, Brazil, (translation in Portuguese of Item no. 3), pps. 498, 2000.
5. M.D. Ercegovic, T. Lang and J. Moreno, *Introduction to Digital Systems.*, New York, NY: John Wiley & Sons, pps. 498, 1999.
6. M.D. Ercegovic and T. Lang. *Division and Square Root: Digit-Recurrence Algorithms and Implementations.* Norwell, MA: Kluwer Academic Publishers, pps. 230, 1994.
7. Conference paper No. 84 reprinted in *Fault-Tolerant Computing - Highlights from 25 Years*, D. Siewiorek, Editor, IEEE Computer Society Press, 1995.
8. Journal papers No. 20, 22, 24, 29, 30, and 37 reprinted in *Computer Arithmetic*, 2 Volumes, E.E. Swartzlander, Jr., Editor, IEEE Computer Society Press, 1990.
9. M.D. Ercegovic and E.E. Swartzlander (Editors), *Proceedings of the 9th IEEE Symposium on Computer Arithmetic*, pps. 247, IEEE Computer Society Press, 1989.
10. M.D. Ercegovic and D. Patel. Reduction Machines. in *High-Level Language Architectures*, Ed. V. Milutinovic, Computer Science, pp.413-429, 1988.
11. M.D. Ercegovic and T. Lang. General Approaches for Achieving High Speed Computations. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.1-28, 1986.
12. M.D. Ercegovic and T. Lang. Vector Processing. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.29-57, 1986.
13. M.D. Ercegovic and T. Lang. *Digital Systems and Hardware/Firmware Algorithms.* New York: J. Wiley & Sons, pps. 838, 1985.

Journal Publications

1. D. Wang, M.D. Ercegovic, and N. Zheng, Design of High-Throughput Fixed-Point Complex Reciprocal/Square-Root Unit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(8):627-631, 2010.
2. M.D. Ercegovic and J.-M. Muller, An Efficient Method for Evaluating Complex Polynomials. *Journal of Signal Processing Systems*, Volume 58, Issue 1, Page 17, Springer 2010, also published online <http://www.springerlink.com/content/5582844402n0t2x1/>

3. Kwak, S., Lee, J.-G., Jung, E.-G., Har, D., Ercegovic, M.D., J.-A. Lee, Exploration of Power-Delay Trade-Offs with Heterogeneous Adders by Integer Linear Programming, *Journal of Circuits, Systems, and Computers*, 18(4):787 - 800 (2009)
4. M.D. Ercegovic and J.-M. Muller, Complex Square Root with Operand Prescaling. *Journal of VLSI Signal Processing*, 49:1930, 2007.
5. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding: Algorithm and Implementation. *Journal of VLSI Signal Processing*, Vol.40, pp.109-123, 2005.
6. Z. Huang and M.D. Ercegovic, High-Performance Low-Power Left-to-Right Array Multiplier Design. *IEEE Trans. Computers*, 54(3):272-283, 2005.
7. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera, Algorithm and Architecture for Logarithm, Exponential, and Powering Computation. *IEEE Trans. Computers*, 53(9):1085-1096, 2004.
8. D. Chen, J. Cong, M.D. Ercegovic, and Z. Huang, Performance-driven mapping for CPLD architectures. *IEEE Trans. on CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp. 1424-1431, October 2003.
9. M.D. Ercegovic and T. Lang, Comments on "A carry-free 54x54-bit multiplier using equivalent bit conversion", *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 1, pp. 160-161, 2003.
10. D. Lau, A. Schneider, M.D. Ercegovic, and J.A. Villasenor, FPGA-based library for on-line signal processing. *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, 28(1-2):129-43, Kluwer Academic Publishers, May-June 2001.
11. M.D. Ercegovic, T. Lang, J.-M. Muller, and A. Tisserand, Reciprocation, Square Root, Inverse Square Root, and Some Elementary Functions Using Small Multipliers. *IEEE Trans. Computers*, 49(7):628-637, 2000.
12. M.D. Ercegovic, L. Imbert, D.W. Matula, J.-M. Muller, and G. Wei, Improving Goldschmidt Division, Square Root, and Square Root Reciprocal. *IEEE Trans. Computers*, 49(7):759-762, 2000.
13. M.R. Stan, A.F. Tenca, and M.D. Ercegovic, Long and Fast Up/Down Counters. *IEEE Trans. Computers*, 47(7):722-735, 1998.
14. J.S. Fernando and M.D. Ercegovic, A Method of Eliminating Oscillations in High-Speed Recursive Digital Filters. *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10):861-864, 1997.
15. M.D. Ercegovic and T. Lang, On Recoding in Arithmetic Algorithms, *J. of VLSI Signal Processing*, 14:283-294, 1996.
16. R. Dionysian and M.D. Ercegovic. Vector Quantization with Variable-Precision Classification. *IEEE Trans. on Image Processing*, 5(11):1528-1538, 1996.
17. R. Dionysian and M.D. Ercegovic, Vector quantization with compressed codebooks. *Image Communications*, 9:79-88, 1996.

18. M. Louie and M.D. Ercegovac. A variable-precision square root implementation on field programmable gate arrays. *The Journal of Supercomputing*, 9:315–336, 1995.
19. M. Louie and M.D. Ercegovac. Implementing division with field programmable gate arrays. *J. of VLSI Signal Processing*, 7:271–285, 1994.
20. M.D. Ercegovac, T. Lang, and P. Montuschi. Very-high radix division with prescaling and selection by rounding. *IEEE Trans. Comput.*, 43(8):909–918, August 1994.
21. J.S. Fernando and M.D. Ercegovac. Conventional and on-line arithmetic designs for high-speed recursive digital filters. *J. of VLSI Signal Processing*, 7:189–197, 1994.
22. M.D. Ercegovac and T. Lang. Multiplication/division/square root module for massively parallel computers. *Integration, the VLSI Journal*, 16:221–234, 1993.
23. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A methodology for performance analysis of parallel computations with looping constructs. *J. of Parallel and Distributed Computing*, 14(3):105–120, March 1992.
24. L. Alkalaj, T. Lang, and M.D. Ercegovac. Architectural support for goal management in flat concurrent Prolog. *Computer*, 25(8):34–47, August 1992.
25. M.D. Ercegovac and T. Lang. On-the-fly rounding. *IEEE Trans. Comput.*, Vol. 41(12):1497–1503, Dec. 1992.
26. M.D. Ercegovac and T. Lang. Module to perform multiplication, division and square root in systolic arrays for matrix computations. *J. Parallel and Distributed Computing*, 11(3):212–221, March 1991.
27. S.-L. Lu and M. D. Ercegovac. Evaluation of two-summands adders implemented in ECDL CMOS differential logic. *IEEE J. of Solid-State Circuits*, 26(6):1152–1160, August 1991.
28. P.K.-G. Tu and M.D. Ercegovac. Gate array implementation of on-line algorithms for floating-point operations. *J. of VLSI Signal Processing*, (3):307–317, 1991.
29. S.-L. Lu and M. D. Ercegovac. A novel CMOS implementation of double-edge-triggered flip-flops. *IEEE Journal of Solid-State Circuits*, 25(4):1008–1009, August 1990.
30. M.D. Ercegovac and T. Lang. Simple radix-4 division with operands scaling. *IEEE Trans. Comput.*, Vol. C-39(9):1204–1207, Sept. 1990.
31. M.D. Ercegovac and T. Lang. Redundant and on-line CORDIC: Application to matrix triangularization and svd. *IEEE Trans. Comput.*, 39(6):725–740, June 1990.
32. M.D. Ercegovac and T. Lang. Radix-4 square root without initial PLA. *IEEE Trans. Comput.*, Vol. C-39(8):1016–1024, Aug. 1990.
33. M.D. Ercegovac and T. Lang. Fast multiplication without carry-propagate addition. *IEEE Trans. Comput.*, C-39(11):1385–1390, November 1990.

34. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A modeling methodology for the analysis of concurrent systems and computations. *Journal of Parallel and Distributed Computing*, 6:568–597, 1989.
35. M.D. Ercegovac and T. Lang. Fast radix-2 division with quotient-digit prediction. *J. of VLSI Signal Processing*, 2(1):169–180, Jan. 1989.
36. M.D. Ercegovac and T. Lang. Binary counter with counting period of one half adder independent of counter size. *IEEE Transactions on Circuits and Systems*, 36(6):924–926, June 1989.
37. M.D. Ercegovac and T. Lang. On-line scheme for computing rotation factors. *J. Parallel and Distributed Computing*, 5(6):209–227, June 1988.
38. M.D. Ercegovac. Heterogeneity in supercomputer architectures. *Parallel Computing*, 7:367–372, September 1988.
39. M.D. Ercegovac and T. Lang. On-the-fly conversion of redundant into conventional representations. *IEEE Trans. Comput.*, Vol. C-36(7):895–897, July 1987.
40. J.L. Gaudiot and M.D. Ercegovac. Performance analysis of variable resolution dataflow systems. *J. of Parallel and Distributed Systems*, November 1985.
41. C.S. Raghavendra, A. Avizienis, and M.D. Ercegovac. Fault-tolerance in binary tree architectures. *IEEE Trans. Comput.*, Vol. C-33(6):568–571, June 1984.
42. O. Watanuki and M. D. Ercegovac. Error analysis of certain floating-point on-line algorithms. *IEEE Trans. Comput.*, C-32(4):352–358, April 1983.
43. V.G. Oklobdzija and M.D. Ercegovac. An on-line square root algorithm. *IEEE Trans. Comput.*, Vol. C-31(1):70–75, Jan. 1982.
44. M.D. Ercegovac. A fast Gray-to-binary code conversion. *Proc. of the IEEE*, 66(4):524–525, April 1978.
45. M.D. Ercegovac. Reply on 'comments on A fast Gray-to binary conversion'. *Proc. of the IEEE*, 67(3):444–445, March 1979.
46. M.D. Ercegovac. A general hardware-oriented method for evaluation of functions and computations in a digital computer. *IEEE Trans. Comput.*, C-26(7):667–680, July 1977.
47. K.S. Trivedi and M.D. Ercegovac. On-line algorithms for division and multiplication. *IEEE Trans. Comput.*, C-26(7):681–687, July 1977.
48. M.D. Ercegovac. Radix-16 evaluation of certain elementary functions. *IEEE Trans. Comput.*, Vol. C-22(6):561–566, June 1973.

Conference Publications

1. P. Kulkarni, P. Gupta, and M.D Ercegovac, Trading Accuracy for Power with an Underdesigned Multiplier Architecture, *Proc. 24th Annual Conference on VLSI Design*, pp. 346-351, 2011.

2. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Combined Division/Square Root Algorithm with Limited Precision Primitives, *Proc. 44rd Asilomar Conference on Signals, Systems and Computers*, 2010.
3. N. Brisebarre, N. Louvet, . Martin-Dorel, J.-M. Muller, A. Panhaleux, and M.D. Ercegovac, Implementing Decimal Floating-Point Arithmetic through Binary: some Suggestions. *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2010*, July 2010.
4. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Algorithm for Square Root with Limited Precision Primitives, *Proc. 43rd Asilomar Conference on Signals, Systems and Computers*, 2009.
5. P. Dormiani, M.D. Ercegovac, and J.-M. Muller, Low Precision Table Based Complex Reciprocal Approximation, *Proc. 43rd Asilomar Conference on Signals, Systems and Computers*, 2009.
6. D. Wang, M.D. Ercegovac, and N. Zheng, A Radix-8 Complex Divider for FPGA Implementation, *Proc. IEEE FPL Conference*, 2009.
7. M.D. Ercegovac and R. McIlhenny, On the design of a Radix 10 online floating-point multiplier, *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, August 2009.
8. D. Wang and M.D. Ercegovac, A Design of Complex Square Root for FPGA Implementation, *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, August 2009 .
9. P.D. Dormiani, M.D. Ercegovac, and J.-M. Muller, Design and Implementation of a Radix-4 Complex Division Unit with Prescaling, *IEEE International Conference on Application-Specific Systems, Architectures and Processors - ASAP 2009*, July 2009.
10. P. Dormiani and M.D. Ercegovac, Design and Implementation of Complex Multiply Add and Other Similar Operators. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XVIII*, Vol. 7074, 12 pps., 2008.
11. M.D. Ercegovac and R. McIlhenny, Design and FPGA Implementation of Radix-10 Algorithm for Division with Limited Precision Primitives. *Proc. 42nd Asilomar Conference on Signals, Systems and Computers*, pp. 1-5, 2008.
12. N. Brisebarre, S. Chevillard, M. D. Ercegovac, J.-M. Muller and S. Torres. An Efficient Method for Evaluating Polynomial and Rational Function Approximations. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 233-238, July 2008.
13. T.Y. Yeh, P. Faloutsos, M.D. Ercegovac, S.J. Patel, and G. Reinman. The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration. 40th Annual IEEE/ACM International Symposium on Microarchitectures, MICRO-07, pp. 394-406, 2007.
14. J-G. Lee, J-A. Lee, B-S. Lee, and M.D. Ercegovac, A Design Method for Heterogeneous Adders, *Proc. ICSS 2007, Lecture Notes in Computer Science 4532*, pp. 121-132, Springer-Verlag, 2007.

15. M.D. Ercegovac. On Digit-by-Digit Methods for Computing of Certain Functions. *Proc. 41st Asilomar Conference on Signals, Systems and Computers*, pp. 338-342, 2007.
16. P. Dormiani and M.D. Ercegovac, ISA Extensions for Online Floating-Point Addition. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, Vol. 6697, 12 pps., 2007.
17. M.D. Ercegovac and J.-M. Muller, Complex Multiply-Add and Other Related Operators. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, Vol. 6697, 12 pps., 2007.
18. M.D. Ercegovac and J.-M. Muller, A Hardware-Oriented Method for Evaluating Complex Polynomials. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 122-127, 2007.
19. M.D. Ercegovac, Omnipresence of Tesla's Work and Ideas. 6th International Symposium Nikola Tesla, pp. 251-56, October 2006.
20. M.D. Ercegovac and J.-M. Muller, Arithmetic Processor for Solving Tridiagonal Systems of Linear Equations. *Proc. 40th Asilomar Conference on Signals, Systems and Computers*, pp. 337-340, 2006.
21. P. Dormiani and M.D. Ercegovac, Interconnection Scheme for Networks of Online Modules. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 631308-1:12, 2006.
22. R. McIlhenny and M.D. Ercegovac, On the Design of an On-line Complex Householder Transform, *Proc. 40th Asilomar Conference on Signals, Systems and Computers*, pp. 318-322, 2006.
23. J.C. Bajard, S. Duquesne, M. Ercegovac, and N. Meloni, Study of RNS representation and modular products summation. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 631304-1:11, 2006.
24. R. McIlhenny and M. D. Ercegovac, On the Design of an On-line Complex Matrix Inversion Unit. *Proc. 39th Asilomar Conference on Signals, Systems and Computers*, pp. 1172-1176, 2005.
25. M. D. Ercegovac, J.-M. Muller, A. Tisserand, Simple Seed Architectures for Reciprocal and Inverse Square Root. *Proc. 39th Asilomar Conference on Signals, Systems and Computers*, pp. 1167-1171, 2005.
26. P. Dormiani, D. Omoto, P. Adharapurapu, and M.D. Ercegovac, A Design of Online Scheme for Evaluation of Multinomials. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, 12 pps., 2005.
27. M.D. Ercegovac and J.-M. Muller, Variable Radix Real and Complex Digit-Recurrence Division. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 316-321, 2005.
28. P. Adharapurapu and M.D. Ercegovac, A Linear-System Operator Based Scheme for Evaluation of Multinomials. *Proc. 17th IEEE Symposium on Computer Arithmetic*, pp. 249-256, 2005.
29. P. Adharapurapu and M.D. Ercegovac, A Composite Arithmetic Scheme for Evaluation of Multinomials. *Proc. 38th Asilomar Conference on Signals, Systems and Computers*, pp. 1889-1893, 2004.

30. R. McIlhenny and M.D. Ercegovic, On the Design of an On-Line Complex FIR Filter. *Proc. 38th Asilomar Conference on Signals, Systems and Computers*, pp. 478-482, 2004.
31. M.D. Ercegovic and J.-M. Muller, Complex Square Root with Operand Prescaling. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2004. (**Best Paper Award**)
32. D. Rennels and M. D. Ercegovic, From the University of Illinois via JPL and UCLA to Vytautas Magnus University - 50 years of computer engineering by Algirdas Avizienis. *IFIP Congress Topical Sessions*. pp. 175-190, 2004.
33. M.D. Ercegovic and J.-M. Muller, Design of a complex divider. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 51-59, 2004.
34. M. D. Ercegovic, Left-to-right squarer with overlapped LS and MS parts. In *Proc. 37th Asilomar Conference on Signals, Systems and Computers*, pp. 1451-1455, 2003.
35. M.D. Ercegovic and J.-M. Muller, Digit-recurrence algorithms for division and square root with limited precision primitives. *Proc. 37th Asilomar Conference on Signals, Systems and Computers*, pp. 1440-1444, 2003.
36. Z. Huang and M.D. Ercegovic, Two-dimensional Signal Gating for Low Power in High-Performance Multipliers. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 499-509, 2003.
37. M.D. Ercegovic and J.-M. Muller, Complex Division with Prescaling of Operands. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2003.
38. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, High-Radix Iterative Algorithm for Powering Computation. *Proc. 16th IEEE Symposium on Computer Arithmetic*, pp. 204-211, 2003.
39. Z. Huang and M.D. Ercegovic, High-performance Left-to-Right Array Multiplier Design. *Proc. 16th IEEE Symposium on Computer Arithmetic*, pp. 4-11, 2003.
40. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, On-Line High-Radix Exponential with Selection by Rounding. *The IEEE International Symposium on Circuits and Systems (ISCAS 2003)*. pp. 121-124, 2003.
41. E.G. Benowitz, M.D. Ercegovic, and F. Fallah, Reducing the Latency of Division Operations with Partial Caching. *Proc. 36th Asilomar Conference on Signals, Systems and Computers*, 2002.
42. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, Analysis of Tradeoffs for the Implementation of a High-Radix Logarithm. *IEEE International Conference on Computer Design: VLSI in Computers and Processors*, pp.132-137, 2002.
43. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 101-110, 2002.

44. Z. Huang and M.D. Ercegovic, Two-dimensional Signal Gating for Low-Power Array Multiplier Design, *The IEEE International Symposium on Circuits and Systems (ISCAS 2002)*. pp. 489-492, vol.1, 2002.
45. Z. Huang and M.D. Ercegovic, Number Representation Optimization for Low-Power Multiplier Design. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, volume 4791, 2002.
46. Z. Huang and M.D. Ercegovic, Low Power Array Multiplier Design by Topology Optimization. In *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, volume 4791, 2002.
47. V. Raghunathan, A. Raghunathan, M. Srivastava, M.B. and M.D. Ercegovic, High-level synthesis with SIMD units. *Proc. ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design*, p.407-13, 2002.
48. J. Vujic, A. Marincic, M.D. Ercegovic, and B. Milovanovic. Nikola Tesla: 145 years of visionary ideas. 5th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service-TELSIKS 2001. Volume 1, 19-21 Sept. 2001 Page(s):323 - 326 vol.1.
49. D. Chen, J. Cong, M.D. Ercegovic, and Z. Huang, Performance-Driven Mapping for CPLD Architectures. In *Proc. ACM/SigDA 9th International Symposium on Field-Programmable Gate Arrays*, pp.39 - 43, February 2001.
50. R. McIlhenny and M.D. Ercegovic, On the Design of On-Line Givens Rotation. In *Proc. 35th Asilomar Conference on Signals, Systems and Computers*, 2001.
51. Z. Huang and M.D. Ercegovic, On Signal-gating Scheme for Low-Power Adders, *Proc. 35th Asilomar Conference on Signals, Systems and Computers*, 2001.
52. Z. Huang and M.D. Ercegovic, FPGA Implementation of Pipelined On-line Scheme for 3-D Vector Normalization, *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 61-70, 2001.
53. M.D. Ercegovic and T. Lang, Division with Limited Precision Primitive Operations. *Proc. 35th Asilomar Conference on Signals, Systems and Computers*, pp. 841-845, 2001.
54. J.M. Fischer and M.D. Ercegovic. A component framework for communication in distributed applications. In *Proceedings 14th International Parallel and Distributed Processing Symposium. IPDPS 2000*, p.647-53, 2000.
55. I. Ferguson and M. D. Ercegovic, The IEEE Rounding for Multiplier with Redundant Operands. In *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1334-8, 2000.
56. M.D. Ercegovic. Left-to-Right Carry-Free Scheme for Computing $ab + cd$. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1330-3, 2000.
57. Z. Huang and M.D. Ercegovic. Effect of Wire Delay on the Design of Prefix Adders in Deep-Submicron Technology. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1713-17, 2000.

58. R. McIlhenny, Z. Huang, K. Wong, A. Schneider, and M.D. Ercegovac. BigSky - A Tool for Mapping Numerically Intensive Computations onto Reconfigurable Hardware. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.394-8, 2000.
59. Bajard, J.C., M.D. Ercegovac, L. Imbert, and F. Rico. Fast Evaluation of Elementary Functions with Combined shift-and-add and Polynomial Methods. *Proc. 4th Conference on Real Numbers and Computers (RNC4)*, Dagstuhl, Germany, 2000.
60. M.D. Ercegovac and T. Lang. On-Line Scheme for Normalizing a 3-D Vector. *Proc. 33rd Asilomar Conference on Signals, Systems and Computers*, pages 1460-1464, 1999.
61. R. McIlhenny and M.D. Ercegovac. On the Design of an On-Line FFT Butterfly Network for FPGAs. *Proc. 33rd Asilomar Conference on Signals, Systems and Computers*, pages 1484-1488, 1999.
62. I. Ferguson and M.D. Ercegovac. A Multiplier with Redundant Operands. *Proc. 33rd Asilomar Conference on Signals, Systems and Computers*, pages 1322-1326, 1999.
63. M.D. Ercegovac, D. Kirovski, M. Potkonjak, Low-power behavioral synthesis optimization using multiple precision arithmetic. *Proceedings 1999 Design Automation Conference*, p.568-73, 1999.
64. A.F. Tenca and M.D. Ercegovac. On the Design of High-Radix On-Line Division for Long Precision. In *Proc. 14th IEEE Symposium on Computer Arithmetic*, pages 59-66, 1999.
65. A.F. Tenca, M.D. Ercegovac and M. Louie. Fast On-Line Multiplication Using LSA Organization. *Proc. SPIE on Image Processing Architectures, Digital Signal Processing*, volume 3807, 1999.
66. M.D. Ercegovac, T. Lang, J.-M. Muller, and A. Tisserand. Reciprocation, Square Root, Inverse Square Root, and Some Elementary Functions using Small Multipliers. *Proc. SPIE on Image Processing Architectures, Digital Signal Processing*, volume 3461, pages 543-554, 1998.
67. R. McIlhenny and M.D. Ercegovac. On-Line Algorithms for Complex Number Arithmetic. *Proc. 32nd Asilomar Conference on Signals, Systems and Computers*, pages 172-176, 1998.
68. M.D. Ercegovac and J.-M. Muller. Fast Evaluation of Functions at Regularly Spaced Points. *Proc. SPIE on Image Processing Architectures, Digital Signal Processing*, volume 3461, pages 555-566, 1998.
69. M. D. Ercegovac, D. Kirovski, G. Mustafa, and M. Potkonjak. Behavioral Synthesis Optimization Using Multiple Precision Arithmetic. *Proc. IEEE ICASSP*, Vol. V, pp.3113-3116, 1998.
70. A.F. Tenca and M.D. Ercegovac. A Variable Long-Precision Arithmetic Unit Design for Reconfigurable Coprocessor Architectures. *IEEE Symposium on Field-Programmable Custom Computing Machines*, pages 216-225, 1998.
71. A.F. Tenca and M.D. Ercegovac. Synchronous Up/Down Binary Counter for LUT FPGAs with Counting Frequency Independent of Counter Size. *FPGA97 - ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pages 159-165, 1997.

72. R. McIlhenny and M.D. Ercegovac. On the Implementation of a Three-Operand Multiplier. *31st Asilomar Conference on Signals, Systems and Computers*, pages 1168-1172, 1997.
73. M.D. Ercegovac and T. Lang Effective Coding for Fast Redundant Adders using the Radix-2 Digit Set $\{0,1,2,3\}$, *31st Asilomar Conference on Signals, Systems and Computers*, pages 1163-1167, 1997.
74. A.F. Tenca and M.D. Ercegovac. A High-Radix Multiplier Design for Variable Long-Precision Computations. *31st Asilomar Conference on Signals, Systems and Computers*, pages 1173-1177, 1997.
75. R. McIlhenny and M.D. Ercegovac. On Using 1-out-of-n Codes for (p,q) Counter Implementations. *30th Asilomar Conference on Signals, Systems and Computers*, pages 187- 191, 1996.
76. C. Fabian and M.D. Ercegovac. Input Synchronization in Low Power CMOS Arithmetic Circuits, *30th Asilomar Conference on Signals, Systems and Computers*, pages 172-176, 1996.
77. A.F. Tenca and M.D. Ercegovac. Design of High-Radix Digit-Slices for On-Line Computations. *Proc. SPIE on High-Speed Computing, Digital Signal Processing, and Filtering using Reconfigurable Logic*, volume 2914, pages 14–25, 1996.
78. M.D. Ercegovac, C. Fabian, and T. Lang. On reducing transition counts in sign detection. *29th Asilomar Conference on Signals, Systems and Computers*, pages 596–599, 1995.
79. M.D. Ercegovac, J.M. Muller, and A. Tisserand. FPGA implementation of polynomial evaluation algorithms. *Proc. SPIE on Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing*, volume 2607, pages 177–188, 1995.
80. M.D. Ercegovac and T. Lang. Sign detection and comparison networks with small number of transitions. *Proc. 12th IEEE Symposium on Computer Arithmetic*, pages 59–66, 1995.
81. M.D. Ercegovac and T. Lang, Low-Power Accumulator (Correlator). *1995 IEEE Symposium on Low Power Electronics*, pages 30–31, San Diego, 1995.
82. M.D. Ercegovac and T. Lang. Reducing transition counts in arithmetic circuits. *1994 IEEE Symposium on Low Power Electronics*, pages 67–68, San Diego, 1994.
83. M.D. Ercegovac and T. Lang. On recoding in arithmetic algorithms. *28th Asilomar Conference on Signals, Systems and Computers*, 1994.
84. M. Louie and M.D. Ercegovac. Multiplication and inner product with field programmable gate arrays. *1994 IEEE Workshop on VLSI Signal Processing*, 1994.
85. M. Louie and M.D. Ercegovac. A variable precision multiplier for field programmable gate arrays. *Proc. 2nd International ACM/SIGDA Workshop on Field-Programmable Gate Arrays*, 1994.
86. J. Fernando and M.D. Ercegovac. A method of eliminating oscillations in high-speed recursive filters. *1994 IEEE Workshop on VLSI Signal Processing*, 1994.

87. M.D. Ercegovac, T. Lang, and P. Montuschi. Very high radix division with selection by rounding and prescaling. In *Proc. 11th IEEE Symposium on Computer Arithmetic*, pages 112–119, 1993.
88. M. Louie and M.D. Ercegovac. On digit-recurrence division implementations for field programmable gate arrays. *Proc. 11th IEEE Symposium on Computer Arithmetic*, pages 202–209, 1993.
89. M. Louie and M.D. Ercegovac. A digit-recurrence square root implementation for field programmable gate arrays. In *Proc. IEEE Workshop on FPGAs for Custom Computing Machines*, pages 178–183, 1993.
90. J.J. Liu and M.D. Ercegovac. ALIAS environment: A design tool for application specific arrays. In *Proc. of the 5th IEEE Symposium on Parallel and Distributed Processing*, pages 504–511, 1993.
91. J.J. Liu and M.D. Ercegovac. Symbolic synthesis of parallel processing systems. In *Proc. 7th International Parallel Processing Symposium*, 1993.
92. J. Fernando and M.D. Ercegovac. On-line arithmetic modules for recursive digital filters. *Proc. 26th Asilomar Conference on Signals, Systems, and Computers*, 1992.
93. J. Fernando and M.D. Ercegovac. Conventional and on-line arithmetic designs for high-speed recursive digital filters. *Proc. IEEE Workshop on VLSI Signal Processing*, pages 81–90, 1992.
94. M.D. Ercegovac and T. Lang. Fast arithmetic for recursive computations. *Proc. IEEE Workshop on VLSI Signal Processing*, pages 14–28, 1992.
95. M. Louie and M. Ercegovac. Mapping division algorithms to field programmable gate arrays. *Proc. 26th Asilomar Conference on Signals, Systems, and Computers*, 1992.
96. D. Le, M. Ercegovac, T. Lang, and J. Moreno. MAMACG: A tool for automatic mapping of matrix algorithms onto mesh array computational graphs. *Proc. 1992 Application Specific Array Processors*, pages 511–525. IEEE Computer Society Press, 1992. Eds. J. Fortes, E. Lee, and T. Meng.
97. M.D. Ercegovac and T. Lang. Multiplication/division module for massively parallel computers. *Proc. SPIE, Advanced Signal Processing Algorithms, Architectures, and Implementations*, pages 110–117, San Diego, 1992.
98. R. Dionysian and M.D. Ercegovac. Variable precision representation for efficient VQ codebook storage. *Proc. of Data Compression Conference DCC'92*, pages 319–328, 1992.
99. M.D. Ercegovac. On-line arithmetic for recurrence problems. *Proc. SPIE, Vol.1566, Advanced Signal Processing Algorithms, Architectures, and Implementations II*, pages 263–274, 1991.
100. P.K. Tu and M.D. Ercegovac. Application of on-line arithmetic algorithms to the SVD computation: Preliminary results. *Proc. 10th IEEE Arithmetic Symposium*, pages 246–255, 1991.
101. M.D. Ercegovac, T. Lang, and P. Montuschi. On the implementation of a parallel algorithm for higher radix division. *Proceedings IEEE COMPEURO '91*, pages 603–607, 1991.

102. R. Dianysian and M.D. Ercegovac. Variable precision linear classifier. *VLSI Signal Processing*, pages 124–131. IEEE Press, 1990. Eds. H.S. Moscovitz, K. Yao and R. Jain.
103. L. Alkalaj, T. Lang, and M.D. Ercegovac. Architectural support for the management of tightly-coupled fine-grain goals in flat concurrent Prolog. *Proc. 17th International Symposium on Computer Architecture*, pages 292–301, 1990.
104. P.K. Tu and M.D. Ercegovac. Gate array implementation of on-line algorithms for floating-point operations. *Proc. 24th Asilomar Conference on Signals Circuits and Computers*, 1990.
105. M.D. Ercegovac and T. Lang. Most-significant-digit-first and on-line arithmetic approaches for the design of recursive filters. *23rd Asilomar Conference on Signals, Systems and Computers*, pages 7–11, 1989.
106. M.D. Ercegovac and T. Lang. Radix-4 square root without initial PLA. *Proc. 9th IEEE Symposium on Computer Arithmetic*, pages 162–168, 1989.
107. M.D. Ercegovac and T. Lang. On-the-fly rounding for division and square root. *Proc. 9th IEEE Symposium on Computer Arithmetic*, pages 169–173, 1989.
108. P. Tu and M.D. Ercegovac. Design of on-line division unit. *Proc. 9th IEEE Symposium on Computer Arithmetic*, pages 42–49, 1989.
109. R.H. Brackert, M.D. Ercegovac, and A. Willson. Design of an on-line multiply-add module for recursive digital filters. *Proc. 9th IEEE Symposium on Computer Arithmetic*, pages 34–41, 1989.
110. M.D. Ercegovac and T. Lang. On-line arithmetic for DSP applications. *Proc. 32nd IEEE Midwest Symposium on Circuits and Systems*, 1989.
111. R.H. Brackert, A.N. Willson, and M.D. Ercegovac. Recursive filter using on-line arithmetic. *Proc. IEEE International Symposium on Circuits and Systems*, pages 1552–1556, 1989.
112. M.D. Ercegovac and T. Lang. Implementation of module combining multiplication, division, and square root. *Proc. IEEE International Symposium on Circuits and Systems*, pages 150–153, 1989.
113. D.R. Greening and M.D. Ercegovac. Using simulation and Markov modeling to select data flow threads. *Proc. of Phoenix Conference on Communications and Computers*, pages 168–175, 1989.
114. M.D. Ercegovac and T. Lang. On-line arithmetic: A design methodology and applications in digital signal processing. *VLSI Signal Processing*, pages 252–263, 1988. Eds. R.W. Brodersen and H.S. Moscovitz.
115. M.D. Ercegovac, T. Lang, and R. Modiri. Implementation of fast radix-4 division with operands scaling. *Proc. IEEE International Conference on Computer Design: VLSI in Computers and Processors*, New York, pages 486–489, 1988.
116. M.D. Ercegovac and T. Lang. Implementation of an SVD processor using redundant CORDIC. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, San Diego, pages 300–313, 1988.

117. M.D. Ercegovac and T. Lang. Implementation of fast angle calculation and rotation using on-line CORDIC. *Proc. 1988 IEEE International Symposium on Circuits and Systems*, Helsinki, Finland, pages 2703-2706, 1988.
118. J.G. Nash, L.W. Chow, M.D. Ercegovac, and T. Lang. Implementation of a serial/parallel multiplier and divider on a systolic chip. *IEEE Asilomar Conference on Signals, Systems, and Computers*, pages 211-216, 1987.
119. M.D. Ercegovac and T. Lang. Fast cosine/sine algorithm using on-line CORDIC. *IEEE Asilomar Conference on Signals, Systems, and Computers*, pages 222-226, 1987.
120. M.D. Ercegovac and T. Lang. Fast radix-4 multiplication without carry-propagate addition. *Proc. ICCD '87 Conference*, New York, pages 654-658, 1987.
121. M.D. Ercegovac, T. Lang, J.G. Nash, and L.P. Chow. An area-time efficient binary divider. *Proc. ICCD '87 Conference*, New York, pages 645-648, 1987.
122. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A methodology for the performance evaluation of distributed computations. *Proc. IFIP Conference on Distributed Processing*, pages 1-14, 1987.
123. M.D. Ercegovac and T. Lang. On-line schemes for computing rotation angles for SVDs. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations*, San Diego, pages 160-169, 1987.
124. M.D. Ercegovac and T. Lang. On-line scheme for computing rotation factors. *Proc. 8th IEEE Symposium on Computer Arithmetic*, pages, 196-203, 1987.
125. P. Tu and M.D. Ercegovac. A radix-4 on-line division algorithm. In *8th IEEE Symposium on Computer Arithmetic*, pages, 1-8, 1987.
126. T.M. Ravi, M.D. Ercegovac, T. Lang, and R.R. Muntz. Static allocation for a dataflow multiprocessor system. *Proc. 2nd International Conference on Supercomputing*, pages 169-178, Santa Clara, 1987.
127. L. Alkalaj, M.D. Ercegovac, and T. Lang. A dynamic memory management policy for fp. *1987 Hawaii International Conference on Systems Science*, pages 1-14, 1987.
128. D. Tullsen and M.D. Ercegovac. Design and implementation of an on-line algorithm. In *Proc. SPIE Conference on Real-Time Signal Processing*, pages 92-99, San Diego, August 1986.
129. D.R. Patel, M. Schlag, and M.D. Ercegovac. vfp: An environment for the multi-level specification, analysis, and synthesis of hardware algorithms. *Proc. Conference on Functional Programming Languages and Computer Architecture*, pages 238-255, Nancy, France, 1985. Springer-Verlag Lecture Notes 201.
130. F. Meshkinpour and M.D. Ercegovac. A functional language for description and design of digital systems: Sequential constructs. *IEEE Proc. of the 22nd ACM/IEEE Design Automation Conference*, pages 238-244, 1985.

131. M.D. Ercegovac and T. Lang. A division algorithm with prediction of quotient digits. *Proc. IEEE 7th Symposium on Computer Arithmetic*, pages 51–56, Urbana, Illinois, 1985.
132. J.L. Gaudiot and M.D. Ercegovac. Performance analysis of a data-flow computer with variable resolution actors. *Proc. of the 1984 International Conference on Distributed Processing*, pages 2-9, 1984.
133. M.D. Ercegovac. On-line arithmetic: An overview. *SPIE Vol. 495 Real-Time Signal Processing VII*, pages 86–93, 1984.
134. M.D. Ercegovac and W.J. Karplus. On a dataflow approach in high-speed simulation of continuous systems. *Proc. International Workshop on High-Level Architecture*, pages 1-8, 1984.
135. J.L. Gaudiot and M.D. Ercegovac. Evaluation of ring communication networks in a data-flow computer. *Proc. of Phoenix Conference on Communications and Computers*, pages 98-105, 1984.
136. M.D. Ercegovac, P.K. Chan, Z. Konstantinovic, T.M. Ravi, and M.D.F. Schlag. Task partitioning, allocation and simulation for a dataflow multi-microprocessor system. *Proc. Summer Computer Simulation Conference*, 1984.
137. J.L. Gaudiot and M.D. Ercegovac. Simulation of a data-flow machine using the SARA system. *ACM/IEEE 21st Design Automation Conference*, pages 485-489, 1984.
138. M.D. Ercegovac, P.K. Chan, and T.M. Ravi. A dataflow multimicroprocessor architecture for high-speed simulation of continuous systems. *Proc. International Workshop on High-Level Architecture*, 1984.
139. M.D. Ercegovac and G.J. Nash. An area-time efficient VLSI design of a radix-4 multiplier. *International Conference on Computer Design - VLSI in Computers*, New York, pages 684-687, 1983.
140. M.D. Ercegovac. A survey of floating-point arithmetic implementations. *Proceedings 1983 SPIE Conference on Real-Time Signal Processing*, pages 60-72, 1983.
141. M.D. Ercegovac and S.L. Lu. A functional language architecture for high-speed digital simulation. *1983 Summer Computer Simulation Conference*, pages 2: 383-387, 1983.
142. T. Lang and M.D. Ercegovac. General approaches for achieving high speed computations. *Proc. 1983 Summer Computer Simulation Conference*, Vancouver, pages 2: 992-1006, 1983.
143. M.D. Ercegovac, D.R. Patel, and T. Lang. Functional language and data flow architectures. *Proc. 1983 Summer Computer Simulation Conference*, Vancouver, pages 2: 1007-1023, 1983.
144. A.L. Grnarov and M.D. Ercegovac. On-line multiplicative normalization. *Proceedings of the 6-th IEEE Symposium on Computer Arithmetic*, Aarhus, Denmark, pages 151-155, 1983.
145. M.D. Ercegovac. A higher-radix division with simple selection of quotient digits. *Proceedings of the 6-th IEEE Symposium on Computer Arithmetic*, Aarhus, Denmark, pages 94-98, 1983.

146. C.S. Raghavendra, A.A. Avizienis, and M.D. Ercegovac. Fault tolerance in binary tree architectures. *1983 International Symposium on Fault-Tolerant Computing*, pages 360-368, Milan, Italy, 1983.
147. M.D. Ercegovac and P.K. Chan. On reducing storage requirements of table-lookup multiplication. *Proc. 16th Asilomar Conference on Circuits, Systems and Computers*, November 8-10 1982.
148. V.G. Oklobdzija and M.D. Ercegovac. Testability enhancement of VLSI using circuit structures. *Proc. IEEE 1982 International Conference on Circuits and Computers*, New York, pages 198-201, 1982.
149. J.L. Gaudiot and M.D. Ercegovac. A scheme for handling arrays in data-flow systems. *Proc. 3rd International conference on Distributed Computer Systems*, pages 724-729, 1982.
150. M.D. Ercegovac. Status and trends in the development of supercomputers in the U.S. *Proc. International Conf. DATASHOW '81*, September 1981.
151. O. Watanuki and M.D. Ercegovac. Floating-point on-line arithmetic: Error analysis. *Proc. 5th IEEE Symposium on Computer Arithmetic*, pages 87-91, 1981.
152. O. Watanuki and M.D. Ercegovac. Floating-point on-line arithmetic: Algorithms. *Proc. 5th IEEE Symposium on Computer Arithmetic*, pages 81-86, 1981.
153. A. Gorji-Sinaki and M.D. Ercegovac. Design of a digit-slice on-line arithmetic unit. *Proc. 5th IEEE Symposium on Computer Arithmetic*, pages 72-80, 1981.
154. C.S. Raghavendra and M.D. Ercegovac. A simulator for on-line arithmetic. *Proc. 5th IEEE Symposium on Computer Arithmetic*, pages 72-80, 1981.
155. M. Feller and M.D. Ercegovac. The queue machines: An organization for parallel computation. *Proc. CONPAR '81, Lecture Notes No. 111*, pages 37-47. Springer-Verlag, 1981.
156. A.L. Grnarov, C.S. Raghavendra, and M.D. Ercegovac. Fast multiplication schemes for microprocessor applications. *Proc. Int. Conf. on Microcomputer Applications to Industrial Control*, 1981.
157. A.L. Grnarov and M.D. Ercegovac. VLSI-oriented iterative networks for array computations. *Proc. 1980 IEEE Conf. on Circuits and Computers*, pages 60-64, 1980.
158. M.D. Ercegovac and A.L. Grnarov. On the performance of on-line arithmetic. *Proc. Int. Conf. on Parallel Processing*, pages 55-62, 1980.
159. M.D. Ercegovac. An on-line square root algorithm. *Proc. of the 4th IEEE Symposium on Computer Arithmetic*, pages 183-189, 1978.
160. M.D. Ercegovac and M. Takata. An arithmetic module for efficient evaluation of functions. *Proc. of the 4th IEEE Symposium on Computer Arithmetic*, pages 190-199, 1978.
161. D.A. Rennels, A. Avizienis, and M.D. Ercegovac. A study of standard building blocks for the design of fault-tolerant distributed computer systems. *Proc. of the FTCS 8*, pages 144-149, 1978.

162. Avizienis, A., Ercegovac, M.D., Lang, T., Sylvain, P., Thomasian, A., "An Investigation of Fault-Tolerant Architecture For Large Scale Numerical Computing", Proc. Conference on High Speed Computer and Algorithm Organization, University of Illinois, Academic Press, pages 159-171, 1977.
163. K.S. Trivedi and M.D. Ercegovac. On-line algorithms for division and multiplication. *Proc. of the 3rd IEEE Symposium on Computer Arithmetic*, pages 161–167, 1975.
164. M.D. Ercegovac. A general method for evaluation of functions and computations in a digital computer. *Proc. of the 3rd IEEE Symposium on Computer Arithmetic*, pages 147–157, 1975.

Submitted for Publication

1. D. Wang, M.D. Ercegovac, and N. Zheng, A Radix-16 Combined Complex Division/Square Root Unit with Operand Prescaling, *IEEE Transactions on Computers*, August 2009.

Published Abstracts

1. R. McIlhenny and M.D. Ercegovac, RAVIOLI - Reconfigurable Arithmetic Variable-Precision Implementation of On-Line Instructions. *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 275-276, 2005. (Extended abstract)
2. A. Schneider, R. McIlhenny, and M.D. Ercegovac BigSky - An On-Line Arithmetic Design Tool for FPGAs. *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2000. (Extended Abstract)
3. D. Lau, A. Schneider, M.D. Ercegovac, and J. Villasenor. FPGA-based Structures for On-Line FFT and DCT. *IEEE Symposium on Field-Programmable Custom Computing Machines*, pages 310-311, 1999. (Extended Abstract)
4. M.D. Ercegovac. An approach in reducing complexity of numerical computations. *Algorithms and Complexity; New Directions and Recent Results*, Carnegie-Mellon University, page 452. Academic Press, 1976. (Abstract).

Patents

G.J. Nash, M.D. Ercegovac, and T. Lang, "Method and Aparatus for Performing Division" U.S. Patent 5,012,439, April 30, 1991.

S.W. Chu, M.D. Ercegovac, K.A. Essenwanger, T. Lang, A.L.S. Sakai, "Digital Phase to Digital Sine and Cosine Amplitude Translator" U.S. Patent 5,774,082 June 30, 1998.

Technical Reports

1. Miloš D. Ercegovac, Tomas Lang On-the-Fly Conversion of Redundant into Conventional Representations 1985 850026
2. Jose Nagib Cotrim Arabe, Miloš D. Ercegovac Symbolic Structural Transformations and Compilation Techniques for FP 1986 860025
3. Leon Alkalaj, Miloš D. Ercegovac, Tomas Lang A Dynamic Memory Management Policy for FP 1986 860026

4. Miloš D. Ercegovac, Tomas Lang Alternative On-the-Fly Conversion of Redundant Into Conventional Representations 1986 860027
5. T. M. Ravi, M. D. Ercegovac, T. Lang, R. R. Muntz Static Allocation For A Data Flow Multiprocessor System 1986 860028
6. Miloš D. Ercegovac, Tomas Lang On-Line Scheme for Computing Rotation Factors 1986 860031
7. Dorab Patel, Martine Schlag, Miloš Ercegovac vFP: An Environment for the Multi-level Specification, Analysis, and Synthesis of Hardware Algorithms 1986 860052
8. T. M. Ravi, M. D. Ercegovac Allocation for the SANDAC Multiprocessor System 1986 860059
9. Miloš D. Ercegovac Multiprocessor System Evaluation and Programming Environment - final report 1986 860066
10. Miloš D. Ercegovac, Tomas Lang Simple Radix-4 Division with Divisor Scaling 1987 870015
11. Alex Kapelnikov, Richard R. Muntz, Miloš D. Ercegovac A Modeling Methodology for the Analysis of Concurrent Systems and Computations 1987 870038
12. Miloš D. Ercegovac, Tomas Lang On-Line Schemes for Computing Rotation Angles for SVDs 1987 870043
13. Miloš D. Ercegovac, Tomas Lang Fast Triangularization By Givens Rotation Using On-Line CORDIC 1987 870045
14. Miloš D. Ercegovac, Tomas Lang Redundant and On-line CORDIC: Application to Matrix Triangularization and SVD 1987 870046
15. Miloš D. Ercegovac, Tomas Lang Fast Multiplication Without Carry Propagate Addition 1987 870047
16. Daniel R. Greening, Miloš D. Ercegovac Identifying and Selecting Sequential Threads in Data Flow Programs 1988 880008
17. Miloš D. Ercegovac, Tomas Lang Binary Counter with Counting Period of One Half Adder Independent of Counter Size 1988 880081
18. Miloš D. Ercegovac, Tomas Lang Radix-4 Square Root Without Initial PLA 1989 890013
19. M. E. Louie, M. D. Ercegovac Linear Sequential Arrays: Pipelining Arithmetic Data Paths 1994 940010
20. M. D. Ercegovac, T. Lang Sign Detection and Comparison Networks with a Small Number of Transitions 1995 950005

**Ph.D. Research
Supervision**

- Z. Huang, *High-Level Optimization Techniques for Low-Power Multiplier Design*, 2003. Magma, Inc.,
- J.-A. Pineiro, *Algorithms and Architectures for Elementary Function Computation*, 2003. University of Santiago de Compostela. Intel Labs - Barcelona.
- R.D. McIlhenny, *Complex Number On-line Arithmetic for Reconfigurable Hardware: Algorithms, Implementations, and Applications*, 2002. Assistant Professor, CalState Northridge (CS)
- A.F. Tenca, *Variable Long-Precision Arithmetic (VLPA) for Reconfigurable Architectures*, 1998. Synopsis
- H. Gerben, *CORDIC for High Performance Numerical Computation*, Member of PhD Committee, EE Department, Univ. of Delft, The Netherlands, 1998.
- J. Harding, *virtualRAID: A Mass Storage Architecture for Out-of-Core Applications*, (co-chair with L. McNamee), 1997. Industry
- D.R. Greening, *Simulated Annealing With Errors*, 1995. Industry
- R. Dionysian, *Variable-Precision Arithmetic for Vector Quantization*, 1994.
- M. F. Aguilar, *Conception et Simulation d'une Machine Massivement Parallele en Grande Precision.*, Member PhD Committee, L'Ecole Normale Superieure de Lyon, France, 1994.
- M. E. Louie, *Variable Precision Arithmetic with Lookup Table Based Field Programmable Gate Arrays*, 1994.
- J. H. Liu, *A Synthesis System for Application Specific Arrays Implementing Matrix Computations*, 1994. Industry
- J. S. Fernando, *Design Alternatives for Recursive Digital Filters Using On-Line Arithmetic*, 1993. AMD
- J.-C. Bajard, *Evaluation de Fonctions dans des Systemes Redondant d'Ecriture des Nombres.*, Member PhD Committee, L'Ecole Normale Superieure de Lyon, France, 1993. Professor, University of Montpellier
- S.-L. Lu, *Asynchronous Arithmetic Structures in Differential CMOS*, 1992. Intel Labs
- C. Kesselman, *Integrating Performance Analysis with Performance Improvement in Parallel Programming*, 1991. USC-ISI
- P. K.-G. Tu, *On-Line Arithmetic Algorithms for Efficient Implementation*, 1990. IBM
- D. R. Patel, *An Applicative Framework for Hardware Synthesis*, 1990. Industry
- L. Alkalaj, *Architectural Support for Concurrent Logic Programming Languages*, (co-chair with T. Lang), 1989. Jet Propulsion Laboratory
- R. Brackert, *Design and Implementation of A High Speed Recursive Digital Filter Using On-Line Arithmetic*, (co-chair with A.N. Wilson, Jr.), 1989. Industry
- M. M. Takata, *Interval-based Timing Simulation Using A Graph Model of Timing Behavior (GMTB)*, 1987. Industry
- S. Kelem, *A Method For The Automatic Translation of Algorithms From A High-Level Language Into Integrated Circuits*, (co-chair with B. Bussell), 1987. Industry
- P. Chan, *On Concurrent Architectures For Simulation of Large-Scale Integrated Digital Circuits*, (co-chair with M. Aoki), 1987. Associate Professor, UC Santa Cruz
- A. Kapelnikov, *Analytic Modeling Methodology For Evaluating The Performance of Distributed Multiple-Computer Systems*, (co-chair with R.M. Muntz, 1987. Industry
- M.D.F. Schlag, *Layout From A Topological Description*, (co-chair with S. Greibach), 1986. Professor, UC Santa Cruz
- J. Arabe, *Compiler Considerations and Run-Time Storage Management For A Functional Programming System*, 1986. Professor and Dean, Univ. of Bello Horizonte, Brazil

J.L. Gaudiot, *Partitioning, Allocation and Scheduling Issues for a Class of Dataflow Multiprocessors*, 1982. Professor and Chair, ECE, UCI
V. Oklobdzija, *Design for Testability of VLSI Structures Through The Use of Circuit Techniques*, 1982. Professor, UC Davis
O. Watanuki, *Floating-Point On-Line Arithmetic For Highly Concurrent Digit-Serial Computation: Application to Mesh Problems*, 1981. Professor, Nagoya University, Japan
A. Gorji-Sinaki, *Error-Coded Algorithms For On-Line Arithmetic*, 1981. Industry

**M.S. Thesis
Research
Supervision**

- D. Lander, *Square Root using Limited Precision Primitive Operations*, August 2006 (co-Chair W. Kaiser, EE Department)
- D. Omoto, *Computing Inference in Bayesian Networks using a Reconfigurable System*, October 2005 (co-Chair W. Kaiser, EE Department)
- E.G. Benowitz, *Reducing the Latency of Division Operations with Partial Caching*, 2002.
- A. Schneider, *BigSky: An On-Line Arithmetic Circuit Generation System*, March 1999.
- D. Le, *MAMACG: A Tool for Automatic Mapping of Matrix Algorithms into Mesh Array Computational Graphs*, March 1993.
- W. Wu, *FLAG: An FP based VLSI Layout Generator*, June 1989.
- D. Greening, *Granularity in Manchester Dataflow Programs*, March 1988.
- A. Dianysian, *Acknowledgement Arc Removal in Data Flow Graphs*, December 1987,
- Mazer, A., *APL Implementation on a Message-based Multiprocessor*, March 1987,
- D. M. Tullsen, *A Very Large Scale Integration Implementation of an On-Line Arithmetic Unit*, June 1986, Report No. CSD-860094.
- T.M. Ravi, *Partitioning and Allocation of Functional Programs for Data Flow Processors*, April 1986, Report No. CSD860063.
- M. Louie, *A Distributed Functional Programming Interpreter*, June 1986.
- L. Alkalaj, *A Uniprocessor Implementation of the FP Functional Language*, April 1986, (co-chair T. Lang), Report No. CSD-860064.
- J. Worley, *A Functional Style Description of Digital Systems*, February 1986, CSD-860054.
- F. Meshkinpour, *On Specification and Design of Digital Systems Using an Applicative Hardware Description Language*, November 1984, Report No. CSD-840046.
- S.L. Lu, *A Compiler for a Functional Programming System*, November 1984, Report No. CSD-840045.
- P. Chan, *A Dataflow Multiprocessor: Programming, Simulation and Performance Prediction*, November 1984, Report No. CSD-840044.
- F. Xiong, *A Functional Language Machine Based on Queues*, November 1984, Report No. CSD-840047.
- J. Kellman, *Concurrent Execution of Functional Languages*, June 1982.
- Y. Afek, *Firmware Specification and Its Silicon Translation*, June 1982.
- F. Tong, *Implementation of Optimizing Pipelines for Data Flow Programs*, December 1981.
- M. Dadseresht, *Design Rule Checking and Verification Based on MOS/LSI Mask Information*, December 1981.
- B. Hunt, *Logic Design Simulation: A Language, Interpreter and Simulator*, June 1981.
- G. Karimi, *On VLSI-Oriented Partitioning of Interconnection Networks for Multi-Microcomputer Systems*, March 1981.
- D. Patel, *A System Organization for Applicative Programming*, December 1980.
- D. Lahti, *Applications of a Functional Programming Language to Hardware Synthesis*, December 1980.
- B. Brode, *An Analysis of a High-Performance System: Potential Improvements to the CRAY-I*, December 1980.
- G. Fucik, *Automated Design of Special-Purpose Processors*, September 1980.
- M. Feller, *A Parallel Queue Organization for High-Speed Computing*, June 1980.
- M.C. Chu, *A Multi-Microprocessor Bit-Slice Organization for Function Evaluation*, September 1979,
- M.M. Takata, *A Design of Modular Arithmetic Unit for Polynomial and Ratio-*

nal Function Evaluation, June 1978.

V.G. Oklobdzija, *An On-Line Higher Radix Square Rooting Algorithm*, June 1978.

**Sponsored
Research**

Online Arithmetic Approach to Floating-Point Operations on Massively Parallel Fixed-Point Units, PI, MICRO - ST Microelectronics, 2006.

Online Arithmetic Approach to Floating-Point Operations on Massively Parallel Fixed-Point Units, PI, MICRO - ST Microelectronics, 2005.

Reducing the Latency of Division Operation, PI, MICRO - Fujitsu Labs, 2001.

Reconfigurable Hardware for Numerically Intensive Computations, PI, MICRO - Raytheon Systems, 2000.

Reconfigurable Hardware for Numerically Intensive Computations, PI, MICRO - Raytheon Systems and Xilinx, 1999.

Reconfigurable Hardware for Numerically Intensive Computations, PI, MICRO - Raytheon Systems and Xilinx, 1998.

Effect of Redundancy in Arithmetic Operations on Processor Cycle Time, Architecture and Implementation, PI, NSF Grant, 1998 - 2000.

Arithmetic Algorithms and Structures for Low-Power Systems, CoPI with T. Lang, UCI, NSF Grant, 1994-1998.

Variable-Precision Arithmetic Structures and Algorithms for Field-Programmable Gate Arrays, PI, MICRO - Xilinx & Virtual Computer Company, 1996-1997.

Arithmetic Algorithms and Structures for Low-Power Systems, PI (T. Lang, UC Irvine, Co-PI), NSF Grant, 1994-1997.

On-Line Arithmetic: From Theoretical Studies to Practical Implementation, Travel Grant, NSF-CNRS France, 1993-1996.

Arithmetic Structures and Algorithms for FPGAs, PI, MICRO/Xilinx, 1992-1993.

Field-Programmable Application-Specific Processor Arrays, PI, MICRO - Xilinx, 1991-1992.

On-Line Arithmetic Algorithms for VLSI Design of Recursive Filters, PI (T. Lang, Co-PI), MICRO - Rockwell, 1990-1991.

Design of Mesh Arrays for Matrix Computations, PI (T. Lang, Co-PI), MICRO - Hughes Aircraft Company, 1990-1991.

Flexible Floating-Point Modules for Wafer Scale Integration, PI (T. Lang, Co-PI), MICRO - TRW, 1989-1990.

Composite Operations Using On-Line Arithmetic for Application-Specific Parallel Architectures: Algorithms, Designs, and Experimental Studies, PI (T. Lang, Co-PI), NSF Grant, 1989-1993.

On-Line Arithmetic Algorithms for VLSI Design, PI (T. Lang, Co-PI), MICRO - Rockwell, 1988-1989.

Effect of Nonuniform Traffic on Multistage Interconnection Networks for Multiprocessors, Co-PI (T. Lang, PI), MICRO - Hughes Aircraft Company, 1987-1988.

Concurrent Architectures and Algorithm Mapping in Digital Signal Processing, PI (T. Lang, Co-PI), MICRO - Hewlett Packard, 1987-1988.

Hot-Spot Problem in Interconnection Networks, Co-PI (T. Lang, PI), MICRO - Hughes Aircraft Company, 1986-1987.

Distributed Machine Intelligence, Co-PI (K. Karplus, PI), Aerojet General, 1985.

On-Line Algorithms and Structures for VLSI, PI, Office of Naval Research, 1984-1987.

Multiprocessing System Evaluation and Programming Environment, PI, Sandia National Labs, 1984-1985.

Specification and Design Methodologies for High-Speed Fault-Tolerant Array Algorithms and Structures in VLSI, Co-PI (A. Avizienis, Co-PI), Office of Naval Research, 1983-1986.

A Data Flow Multi-Purpose Processor for High Speed Digital Simulation, PI (W. Karplus, Co-PI), NASA, 1982-1984.

A High Level Language Approach to Custom Chip Layout Design, PI, (L. Mc-Namee, Co-PI), MICRO/Rockwell, 1982-1985.
Data Flow Computing Approach in High-Speed Digital Simulation, PI (W. Karplus, Co-PI), NASA, 1980-1982.
Research in Distributed Processing, Co-PI (A. Avizienis, PI), Office of Naval Research, 1979-1983.
Methodology for the Synthesis of Information Processing Systems, Co-PI (G. Estrin, PI), DOE, 1978-1983.
Fault-Tolerant Computing, (A. Avizienis, PI), NSF Grant, 1975-1978.