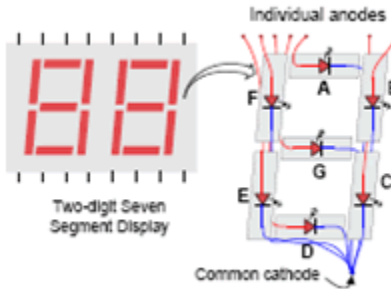


CS m51A: Logic Design of Digital Systems
UCLA Computer Science Department
Fall 2009

Project 1 revised – Combinational Systems
Due Wednesday, October 28, 2009 12:00 Noon Sharp

Provide a design for a decoder that displays a 4-bit binary number (with value 0-15) on 7-segment LED displays.



The binary to 7-segment LED decoder has four 1-bit inputs In_3 , In_2 , In_1 , In_0 , and seven 1-bit outputs A, B, C, D, E, F, G, for controlling the seven segment of the LED display as shown in the figure. Based on the input values the decoder will illuminate the correct segments of the LED display to output 4-bit binary number. For example, to display a zero on one of the displays, the output ABCDEFG = 1111110. This illuminates all LED segments except the middle segment, thereby displaying the digit 0.

The binary to 7-segment LED decoder will have one additional output, to control which of the two 7-segment LED displays will be illuminated. Only one 7-segment LED display can be illuminated at any given time, and your design should include a 1-bit SegSel output to control which display to use. Assume you are given a signal that oscillates between 0 and 1, at a rate faster than what human eyes can detect.

You can only use gates, multiplexers, and modules that you design. For full credit, you must use a hierarchical design.

Materials to Turn in

1. Final Design
2. Cleanly presented material demonstrating your design process

Grading

- Readability – 10%
- Correctness – 60%
- Design Quality – 20%
- Design Process Demonstration – 10%