

Curriculum Vitae

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Education: Ph.D. degree (1975) and M.S. degree (1972) in Computer Science, University of Illinois, Urbana-Champaign, Illinois; B.S. degree (1965) in Electrical Engineering, University of Belgrade, Belgrade, Yugoslavia.

Ph.D. Dissertation: *A General Method for Evaluation of Functions and Computations in a Digital Computer* (U. of Illinois, DCS Technical Report No. 750, 1975).

Ph.D. Committee: James E. Robertson (Chair), David J. Kuck, Chuang L. (Dave) Liu, Donald B. Gillies, and Ahmed Sameh.

Professional Experience: Professor (1984- present), Computer Science Department, HSSEAS, UCLA; Department Chair (9/1/2000 - 6/30/2005); Vice-Chair (Graduate Programs) (1995 - 1998, 1988 - 1994, 1982-1986); Vice-Chair (Industrial Relations) (1998-1999); Associate Professor (1979-1984); Assistant Professor (1975-1979); Research Engineer (1966-1970), Institute for Automation and Telecommunications "M.Pupin," (Digital Laboratory), Belgrade, Yugoslavia; Assistant Engineer (1965-1966), Brown Boveri Co., Telecommunications, Baden, Switzerland; Consultant to: Hughes Research Laboratories, (1979-1990); Jet Propulsion Laboratory, (1978-82); U.S. government and industrial organizations (1975 - present); GMD Institute (German government), (1984-88). Hughes Aircraft Company, (1988 - 1997).

Research Theory and design of computer arithmetic algorithms: emphasis on fast division, square root and multiplication; design of fast floating-point units; complex arithmetic; on-line arithmetic, most-significant-digit-first algorithms, and composite algorithms; arithmetic structures for low power; application-specific numerical processors; reconfigurable gate arrays (FPGAs) and systems; functional (applicative) languages and architectures; digital design.

Teaching UCLA Computer Science Department: *Logic Design of Digital Systems* (CS51A), *Computer Systems Architecture* (CS151B), *Design of Digital Systems - Elective* (CS151C), *Advanced Computer Architecture* (CS251A), *Parallel Computer Architecture* (CS251B), *Arithmetic Algorithms and Processors* (CS252A), *Special*

Topics in High-Speed Computing (CS259 - Seminar);
UCLA Extension: *High-Speed Computer Organization: Super Machines and Low-Cost Systems*, Short Course, (1979 - 1986).

Membership and Professional Services Foreign Member, Serbian Academy of Sciences and Arts, (2003 - present);
Fellow IEEE (2003 - present);
IEEE Computer Society (1975 - present); IEEE Technical Committee for VLSI for Signal Processing;
ACM (1975 - present); SigARCH;
Nikola Tesla Memorial Society, Science Committee (1985 - present);
UCLA Engineer Advisory Board, 2001 - 2004; Chancellor's Advisory Board for the Crump Institute (UCLA Medical School) (1985 - 1995);
IEEE Transactions on Computers, Editorial Board (1988-1992);
Journal of Parallel and Distributed Computing, Editorial Board (1986-1993);
Program Committee of the IEEE Symposium on Computer Arithmetic (1978 - present); General Chair (1978); Program Co-chair (1989);
Chair, IEEE Steering Committee on Computer Arithmetic (1999 - 2001);
Member, IEEE Steering Committee on Computer Arithmetic (1999 - present);
Member, Asilomar Conference on Signals, Systems and Computers, Steering Committee (2004 - present);
Session Chair, ASILOMAR Conference, (1986, 2004, 2006, 2007).
Session Chair, SPIE Conference, (1999-2001, 2003, 2004).
Member, Technical Program Committee, RNC'5 (Real Numbers and Computers), 2003;
Session Chair, SPIE Conference, (1999-2001, 2003, 2004);
Member, Technical Program Committee, FCCM, 2007 - present.

Invited Seminars and Panels

- Getting More from Less: Trends in Computer Architectures, Serbian Academy of Sciences and Arts, Belgrade, September 19, 2007;
- Omnipresence of Tesla's Work and Ideas, Simon Fraser University, Burnaby, Canada, November 17, 2006;
- Omnipresence of Tesla's Work and Ideas, Serbian Academy of Sciences and Arts, Belgrade, October 18, 2006;
- Arithmetic Approaches to Bayesian Network Computations, Intel-Barcelona Lab, July 8, 2005;
- On-line Arithmetic, STMicroelectronics Lab, San Diego, August 11, 2004.
- New Models for Computer Engineering Programs, CRA Conference at Snowbird, July 12, 2004.
- Complex Arithmetic, Microsoft Research Lab, April 21, 2004;
- Fast Low-Power Multipliers, EE Department, University of Belgrade, Serbia, June 2003;
- Complex Division with Prescaling of Operands, ECE Department, University of Wisconsin - Madison, March 2003.
- Fast Arithmetic, ECE Department, George Washington University, Washington, D.C., March 2001.
- Seminar on Nikola Tesla, UC Berkeley, 2000.
- Reconfigurable Arithmetic Seminar, University of Provence, Marseilles, France, June 1999.
- Online Algorithms, Symposium on CORDIC, Technical University, Delft, Holland, March 1998.
- Redundant Arithmetic, Seminar, University of Provence, Marseilles, France, June 1998.
- Online Arithmetic, 12th Symposium on Weak Arithmetic, Metz, France, 1996.

- Approaches to Fast Arithmetic, Real Numbers and Computers, St. Etienne, France, 1995.
- Low-Power Arithmetic, University of California at Los Angeles, Computer Science Department Seminar, 1994.
- Arithmetic for Recursive Filters, Rockwell International Science Center, Thousand Oaks, May 1993.
- Online Arithmetic: Design Methodology and Application, 1992 IEEE Workshop on VLSI Signal Processing, Napa, 1992.
- Fast Arithmetic, **Distinguished Speaker**, EE Department, UC San Diego, 1991.
- On-Line Arithmetic, Ecole Superieure Normal, Lyon, France, 1991.
- Application-Specific Arithmetic Approaches, University of California at Los Angeles, Computer Science Department Seminar, 1990.
- Composite Arithmetic, University of California at Santa Cruz, Computer Science Program Seminar, 1990.
- Vector Processors, ETAN Advanced Simulation Seminar, Dubrovnik, 1990.
- High-Performance Computer Architectures, Lecture Series, Institute M. Pupin, Belgrade, 1989.
- Supercomputers, Annual Computer Society Conference, Rio de Janeiro, Brazil, 1988.
- Redundant Arithmetic, Memorial University, New Foundland, Canada, 1988.
- Fast Arithmetic, USC, EE & Systems Department Seminar, 1987.
- Parallel Architectures, Eidgenossische Technische Hochschule (ETH) Seminar, Zuerich, Switzerland, 1987.
- Supercomputer Architectures, Technical University of Berlin Seminar, 1986.
- On-Line Arithmetic and Dataflow Architectures, University of Utah, Computer Science Department Seminar, 1985.
- High-Performance Architectures, Gesellschaft fuer Mathematische Dataverarbeitung, St.Augustin-Bonn, Germany, 1984;.
- On-Line Arithmetic Algorithms, Yale University, Computer Science Department Seminar, 1983.
- Evaluation of Polynomials and Rational Functions, Ecole Superieure d'Electrotechnique et Electronique Seminar, Paris, 1983.
- Low-Cost Processors, Special Libraries Association, Los Angeles, 1982.
- Panel, IEEE Workshop on Computer Elements, Phoenix, 1982.
- Approaches to High-Performance Architectures, Invited Speaker DATASHOW'81, Tokyo, 1981.
- On Supercomputer Architectures, Institute for Automation "M.Pupin," Belgrade, 1981.
- Dataflow Architectures, Electrical Engineering Department, University of Belgrade, 1981.
- Floating-Point On-Line Arithmetic, University of Michigan, 1980.
- Short Course on Computer Organization, BM Santa Teresa Labs, 1979.
- A Method for Evaluating Rational Approximations, ACM SIGNUM Los Angeles Chapter Seminar, 1978.
- Panel, MIT Data-Flow Workshop, 1977; MIT Data-Flow Workshop, 1978.
- Online Iterative Networks, University of Michigan, Electrical and Computer Engineering, 1976.
- Digital Arithmetic - Some New Results, Electrical Engineering Department, University of Belgrade, 1976.

Awards

Best paper award: M.D. Ercegovac and J.-M. Muller, Complex Square Root with Operand Prescaling. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2004.

Foreign Member of the Serbian Academy of Sciences and Arts, for contributions to theory and practice of digital arithmetic, 2003.

IEEE Fellow, for contributions to theory and practice of digital arithmetic, 2003.

NASA Certificate of Recognition for technical contributions to fault-tolerant computer systems, 1980.

Books, Chapters in Books, and Editorships

1. M.D. Ercegovic and T. Lang. *Digital Arithmetic* Morgan Kaufmann Publishers - an Imprint of Elsevier Science, San Francisco, 2004.
2. M.D. Ercegovic, T. Lang and J. Moreno, *Introduction to Digital Systems.*, John Wiley & Sons, (translation in Chinese), pps. 498, 2002.
3. M.D. Ercegovic, T. Lang and J. Moreno, *Introducao aos Sistemas Digitais.*, Porto Alegre, Brazil, (translation in Portuguese of Item no. 3), pps. 498, 2000.
4. M.D. Ercegovic, T. Lang and J. Moreno, *Introduction to Digital Systems.*, New York, NY: John Wiley & Sons, pps. 498, 1999.
5. M.D. Ercegovic and T. Lang. *Division and Square Root: Digit-Recurrence Algorithms and Implementations.* Norwell, MA: Kluwer Academic Publishers, pps. 230, 1994.
6. Conference paper No. 84 reprinted in *Fault-Tolerant Computing - Highlights from 25 Years*, D. Siewiorek, Editor, IEEE Computer Society Press, 1995.
7. Journal papers No. 20, 22, 24, 29, 30, and 37 reprinted in *Computer Arithmetic*, 2 Volumes, E.E. Swartzlander, Jr., Editor, IEEE Computer Society Press, 1990.
8. M.D. Ercegovic and E.E. Swartzlander (Editors), *Proceedings of the 9th IEEE Symposium on Computer Arithmetic*, pps. 247, IEEE Computer Society Press, 1989.
9. M.D. Ercegovic and D. Patel. Reduction Machines. in *High-Level Language Architectures*, Ed. V. Milutinovic, Computer Science, pp.413-429, 1988.
10. M.D. Ercegovic and T. Lang. General Approaches for Achieving High Speed Computations. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.1-28, 1986.
11. M.D. Ercegovic and T. Lang. Vector Processing. in *Supercomputers*, Ed. S. Fernbach, North Holland, pp.29-57, 1986.
12. M.D. Ercegovic and T. Lang. *Digital Systems and Hardware/Firmware Algorithms.* New York: J. Wiley & Sons, pps. 838, 1985.

Journal Publications

1. M.D. Ercegovic and J.-M. Muller, Complex Square Root with Operand Prescaling. *Journal of VLSI Signal Processing*, 49:1930, 2007.
2. J.-A. Pineiro, M.D. Ercegovic. and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding: Algorithm and Implementation. *Journal of VLSI Signal Processing*, Vol.40, pp.109-123, 2005.
3. Z. Huang and M.D. Ercegovic, High-Performance Low-Power Left-to-Right Array Multiplier Design. *IEEE Trans. Computers*, 54(3):272-283, 2005.

4. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera, Algorithm and Architecture for Logarithm, Exponential, and Powering Computation. *IEEE Trans. Computers*, 53(9):1085-1096, 2004.
5. D. Chen, J. Cong, M.D. Ercegovic, and Z. Huang, Performance-driven mapping for CPLD architectures. *IEEE Trans. on CAD of Integrated Circuits and Systems*, Vol. 22, No. 10, pp. 1424-1431, October 2003.
6. M.D. Ercegovic and T. Lang, Comments on "A carry-free 54x54-bit multiplier using equivalent bit conversion", *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 1, pp. 160-161, 2003.
7. D. Lau, A. Schneider, M.D. Ercegovic, and J.A. Villasenor, FPGA-based library for on-line signal processing. *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, 28(1-2):129-43, Kluwer Academic Publishers, May-June 2001.
8. M.D. Ercegovic, T. Lang, J.-M. Muller, and A. Tisserand, Reciprocation, Square Root, Inverse Square Root, and Some Elementary Functions Using Small Multipliers. *IEEE Trans. Computers*, 49(7):628-637, 2000.
9. M.D. Ercegovic, L. Imbert, D.W. Matula, J.-M. Muller, and G. Wei, Improving Goldschmidt Division, Square Root, and Square Root Reciprocal. *IEEE Trans. Computers*, 49(7):759-762, 2000.
10. M.R. Stan, A.F. Tenca, and M.D. Ercegovic, Long and Fast Up/Down Counters. *IEEE Trans. Computers*, 47(7):722-735, 1998.
11. J.S. Fernando and M.D. Ercegovic, A Method of Eliminating Oscillations in High-Speed Recursive Digital Filters. *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, 44(10):861-864, 1997.
12. M.D. Ercegovic and T. Lang, On Recoding in Arithmetic Algorithms, *J. of VLSI Signal Processing*, 14:283-294, 1996.
13. R. Dionysian and M.D. Ercegovic. Vector Quantization with Variable-Precision Classification. *IEEE Trans. on Image Processing*, 5(11):1528-1538, 1996.
14. R. Dionysian and M.D. Ercegovic, Vector quantization with compressed codebooks. *Image Communications*, 9:79-88, 1996.
15. M. Louie and M.D. Ercegovic. A variable-precision square root implementation on field programmable gate arrays. *The Journal of Supercomputing*, 9:315-336, 1995.
16. M. Louie and M.D. Ercegovic. Implementing division with field programmable gate arrays. *J. of VLSI Signal Processing*, 7:271-285, 1994.
17. M.D. Ercegovic, T. Lang, and P. Montuschi. Very-high radix division with prescaling and selection by rounding. *IEEE Trans. Comput.*, 43(8):909-918, August 1994.
18. J.S. Fernando and M.D. Ercegovic. Conventional and on-line arithmetic designs for high-speed recursive digital filters. *J. of VLSI Signal Processing*, 7:189-197, 1994.
19. M.D. Ercegovic and T. Lang. Multiplication/division/square root module for massively parallel computers. *Integration, the VLSI Journal*, 16:221-234, 1993.

20. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A methodology for performance analysis of parallel computations with looping constructs. *J. of Parallel and Distributed Computing*, 14(3):105–120, March 1992.
21. L. Alkalaj, T. Lang, and M.D. Ercegovac. Architectural support for goal management in flat concurrent Prolog. *Computer*, 25(8):34–47, August 1992.
22. M.D. Ercegovac and T. Lang. On-the-fly rounding. *IEEE Trans. Comput.*, Vol. 41(12):1497–1503, Dec. 1992.
23. M.D. Ercegovac and T. Lang. Module to perform multiplication, division and square root in systolic arrays for matrix computations. *J. Parallel and Distributed Computing*, 11(3):212–221, March 1991.
24. S.-L. Lu and M. D. Ercegovac. Evaluation of two-summands adders implemented in ECDL CMOS differential logic. *IEEE J. of Solid-State Circuits*, 26(6):1152–1160, August 1991.
25. P.K.-G. Tu and M.D. Ercegovac. Gate array implementation of on-line algorithms for floating-point operations. *J. of VLSI Signal Processing*, (3):307–317, 1991.
26. S.-L. Lu and M. D. Ercegovac. A novel CMOS implementation of double-edge-triggered flip-flops. *IEEE Journal of Solid-State Circuits*, 25(4):1008–1009, August 1990.
27. M.D. Ercegovac and T. Lang. Simple radix-4 division with operands scaling. *IEEE Trans. Comput.*, Vol. C-39(9):1204–1207, Sept. 1990.
28. M.D. Ercegovac and T. Lang. Redundant and on-line CORDIC: Application to matrix triangularization and svd. *IEEE Trans. Comput.*, 39(6):725–740, June 1990.
29. M.D. Ercegovac and T. Lang. Radix-4 square root without initial PLA. *IEEE Trans. Comput.*, Vol. C-39(8):1016–1024, Aug. 1990.
30. M.D. Ercegovac and T. Lang. Fast multiplication without carry-propagate addition. *IEEE Trans. Comput.*, C-39(11):1385–1390, November 1990.
31. A. Kapelnikov, R.R. Muntz, and M.D. Ercegovac. A modeling methodology for the analysis of concurrent systems and computations. *Journal of Parallel and Distributed Computing*, 6:568–597, 1989.
32. M.D. Ercegovac and T. Lang. Fast radix-2 division with quotient-digit prediction. *J. of VLSI Signal Processing*, 2(1):169–180, Jan. 1989.
33. M.D. Ercegovac and T. Lang. Binary counter with counting period of one half adder independent of counter size. *IEEE Transactions on Circuits and Systems*, 36(6):924–926, June 1989.
34. M.D. Ercegovac and T. Lang. On-line scheme for computing rotation factors. *J. Parallel and Distributed Computing*, 5(6):209–227, June 1988.
35. M.D. Ercegovac. Heterogeneity in supercomputer architectures. *Parallel Computing*, 7:367–372, September 1988.
36. M.D. Ercegovac and T. Lang. On-the-fly conversion of redundant into conventional representations. *IEEE Trans. Comput.*, Vol. C-36(7):895–897, July 1987.

37. J.L. Gaudiot and M.D. Ercegovac. Performance analysis of variable resolution dataflow systems. *J. of Parallel and Distributed Systems*, November 1985.
38. C.S. Raghavendra, A. Avizienis, and M.D. Ercegovac. Fault-tolerance in binary tree architectures. *IEEE Trans. Comput.*, Vol. C-33(6):568–571, June 1984.
39. O. Watanuki and M. D. Ercegovac. Error analysis of certain floating-point on-line algorithms. *IEEE Trans. Comput.*, C-32(4):352–358, April 1983.
40. V.G. Oklobdzija and M.D. Ercegovac. An on-line square root algorithm. *IEEE Trans. Comput.*, Vol. C-31(1):70–75, Jan. 1982.
41. M.D. Ercegovac. A fast Gray-to-binary code conversion. *Proc. of the IEEE*, 66(4):524–552, April 1978.
42. M.D. Ercegovac. Reply on 'comments on A fast Gray-to binary conversion'. *Proc. of the IEEE*, 67(3):444–445, March 1979.
43. M.D. Ercegovac. A general hardware-oriented method for evaluation of functions and computations in a digital computer. *IEEE Trans. Comput.*, C-26(7):667–680, July 1977.
44. K.S. Trivedi and M.D. Ercegovac. On-line algorithms for division and multiplication. *IEEE Trans. Comput.*, C-26(7):681–687, July 1977.
45. M.D. Ercegovac. Radix-16 evaluation of certain elementary functions. *IEEE Trans. Comput.*, Vol. C-22(6):561–566, June 1973.

Conference Publications

1. T.Y. Yeh, P. Faloutsos, M.D. Ercegovac, S.J. Patel, and G. Reinman. The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration. International Symposium on Microarchitectures, MICRO-07, 2007.
2. M.D. Ercegovac. On Digit-by-Digit Methods for Computing of Certain Functions. *Proc. 41st Asilomar Conference on Signals, Systems and Computers*, pp. xx, 2007.
3. P. Dormiani and M.D. Ercegovac, ISA Extensions for Online Floating-Point Addition. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. xx, 2007.
4. M.D. Ercegovac and J.-M. Muller, Complex Multiply-Add and Other Related Operators. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. xxx, 2007.
5. M.D. Ercegovac and J.-M. Muller, A Hardware-Oriented Method for Evaluating Complex Polynomials. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. xx-xx, 2007.
6. M.D. Ercegovac, Omnipresence of Tesla's Work and Ideas. 6th International Symposium Nikola Tesla, pp. 251-56, October 2006.
7. M.D. Ercegovac and J.-M. Muller, Arithmetic Processor for Solving Tridiagonal Systems of Linear Equations. *Proc. 40th Asilomar Conference on Signals, Systems and Computers*, pp. 337-340, 2006.

8. P. Dormiani and M.D. Ercegovac, Interconnection Scheme for Networks of Online Modules. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 631308-1:12, 2006.
9. R. McIlhenny and M.D. Ercegovac, On the Design of an On-line Complex Householder Transform, *Proc. 40th Asilomar Conference on Signals, Systems and Computers*, pp. 318-322, 2006.
10. J.C. Bajard, S. Duquesne, M. Ercegovac, and N. Meloni, Study of RNS representation and modular products summation. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 631304-1:11, 2006.
11. M. D. Ercegovac, J.-M. Muller, A. Tisserand, Simple Seed Architectures for Reciprocal and Inverse Square Root. *Proc. 39th Asilomar Conference on Signals, Systems and Computers*, pp. 1167-1171, 2005.
12. R. McIlhenny and M. D. Ercegovac, On the Design of an On-line Complex Matrix Inversion Unit. *Proc. 39th Asilomar Conference on Signals, Systems and Computers*, pp. 1172-1176, 2005.
13. P. Dormiani, D. Omoto, P. Adharapurapu, and M.D. Ercegovac, A Design of Online Scheme for Evaluation of Multinomials. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, 12 pps., 2005.
14. M.D. Ercegovac and J.-M. Muller, Variable Radix Real and Complex Digit-Recurrence Division. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 316-321, 2005.
15. P. Adharapurapu and M.D. Ercegovac, A Linear-System Operator Based Scheme for Evaluation of Multinomials. *Proc. 17th IEEE Symposium on Computer Arithmetic*, pp. 249-256, 2005.
16. R. McIlhenny and M.D. Ercegovac, RAVIOLI - Reconfigurable Arithmetic Variable-Precision Implementation of On-Line Instructions. *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 275-276, 2005. (Poster)
17. P. Adharapurapu and M.D. Ercegovac, A Composite Arithmetic Scheme for Evaluation of Multinomials. *Proc. 38th Asilomar Conference on Signals, Systems and Computers*, pp. 1889-1893, 2004.
18. R. McIlhenny and M.D. Ercegovac, On the Design of an On-Line Complex FIR Filter. *Proc. 38th Asilomar Conference on Signals, Systems and Computers*, pp. 478-482, 2004.
19. M.D. Ercegovac and J.-M. Muller, Complex Square Root with Operand Prescaling. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2004. (**Best Paper Award**)
20. M.D. Ercegovac and J.-M. Muller, Design of a complex divider. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 51-59, 2004.
21. D. Rennels and M. D. Ercegovac, From the University of Illinois via JPL and UCLA to Vytautas Magnus University - 50 years of computer engineering by Algirdas Avizienis. *IFIP Congress Topical Sessions*. pp. 175-190, 2004.

22. M. D. Ercegovic, Left-to-right squarer with overlapped LS and MS parts. In *Proc. 37th Asilomar Conference on Signals, Systems and Computers*, pp. 1451-1455, 2003.
23. M.D. Ercegovic and J.-M. Muller, Digit-recurrence algorithms for division and square root with limited precision primitives. *Proc. 37th Asilomar Conference on Signals, Systems and Computers*, pp. 1440-1444, 2003.
24. Z. Huang and M.D. Ercegovic, Two-dimensional Signal Gating for Low Power in High-Performance Multipliers. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, pp. 499-509, 2003.
25. M.D. Ercegovic and J.-M. Muller, Complex Division with Prescaling of Operands. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 293-303, 2003.
26. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, High-Radix Iterative Algorithm for Powering Computation. *Proc. 16th IEEE Symposium on Computer Arithmetic*, pp. 204-211, 2003.
27. Z. Huang and M.D. Ercegovic, High-performance Left-to-Right Array Multiplier Design. *Proc. 16th IEEE Symposium on Computer Arithmetic*, pp. 4-11, 2003.
28. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, On-Line High-Radix Exponential with Selection by Rounding. *The IEEE International Symposium on Circuits and Systems (ISCAS 2003)*. pp. 121-124, 2003.
29. J.-A. Pineiro, M.D. Ercegovic, and J.D Bruguera, Analysis of Tradeoffs for the Implementation of a High-Radix Logarithm. *IEEE International Conference on Computer Design: VLSI in Computers and Processors*, pp.132-137, 2002.
30. Z. Huang and M.D. Ercegovic, Two-dimensional Signal Gating for Low-Power Array Multiplier Design, *The IEEE International Symposium on Circuits and Systems (ISCAS 2002)*. pp. 489-492, vol.1, 2002.
31. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding. *IEEE International Conference on Application-Specific Systems, Architectures and Processors*, pp. 101-110, 2002.
32. E.G. Benowitz, M.D. Ercegovic, and F. Fallah, Reducing the Latency of Division Operations with Partial Caching. *Proc. 36th Asilomar Conference on Signals, Systems and Computers*, 2002.
33. J.-A. Pineiro, M.D. Ercegovic, and J.D. Bruguera. Analysis of the Tradeoffs for the Implementation of a High-Radix Logarithm. *International Conference on Computer Design - ICCD*, Freiburg, Germany, September 2002.
34. Z. Huang and M.D. Ercegovic, Low Power Array Multiplier Design by Topology Optimization. In *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, volume 4791, 2002.
35. Z. Huang and M.D. Ercegovic, Number Representation Optimization for Low-Power Multiplier Design. *Proc. SPIE on Advanced Signal Processing Algorithms, Architectures, and Implementations XII*, volume 4791, 2002.

36. J.-A. Pineiro, M.D. Ercegovac, and J.D. Bruguera, High-Radix Logarithm with Selection by Rounding. *Proc. IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, p. 101-110, 2002.
37. V. Raghunathan, A. Raghunathan, M. Srivastava, M.B. and M.D. Ercegovac, High-level synthesis with SIMD units. *Proc. ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design*, p.407-13, 2002.
38. M.D. Ercegovac and T. Lang, Division with Limited Precision Primitive Operations. *Proc. 35th Asilomar Conference on Signals, Systems and Computers*, pp. 841-845, 2001.
39. M.D. Ercegovac. Left-to-Right Carry-Free Scheme for Computing $ab + cd$. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1330-3, 2000.
40. R. McIlhenny, Z. Huang, K. Wong, A. Schneider, and M.D. Ercegovac. BigSky - A Tool for Mapping Numerically Intensive Computations onto Reconfigurable Hardware. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.394-8, 2000.
41. Z. Huang and M.D. Ercegovac. Effect of Wire Delay on the Design of Prefix Adders in Deep-Submicron Technology. *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1713-17, 2000.
42. I. Ferguson and M. D. Ercegovac, The IEEE Rounding for Multiplier with Redundant Operands. In *Proc. 34th Asilomar Conference on Signals, Systems and Computers*, pp.1334-8, 2000.
43. J.M. Fischer and M.D. Ercegovac. A component framework for communication in distributed applications. In *Proceedings 14th International Parallel and Distributed Processing Symposium. IPDPS 2000*, p.647-53, 2000.
44. A. Schneider, R. McIlhenny, and M.D. Ercegovac BigSky - An On-Line Arithmetic Design Tool for FPGAs. (Extended Abstract) *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2000.
45. Bajard, J.C., M.D. Ercegovac, L. Imbert, and F. Rico. Fast Evaluation of Elementary Functions with Combined shift-and-add and Polynomial Methods. *Proc. 4th Conference on Real Numbers and Computers (RNC4)*, Dagstuhl, Germany, 2000.
46. M.D. Ercegovac and T. Lang. On-Line Scheme for Normalizing a 3-D Vector. *Proc. 33rd Asilomar Conference on Signals, Systems and Computers*, pages 1460-1464, 1999.
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